

MODEL NAME : *QLM00*

PCB NO : *LA-7841P (DA *****)*

BOM P/N : *TBD*

Dell/Compal Confidential

Schematic Document

Phantom(Chief River)

Ivy Bridge ULV(BGA1023) + Panther Point

DISCRETE VGA N13P-GV(optimus)

2012-01-19

Rev: 1.0 (X04)

@ : Nopop Component

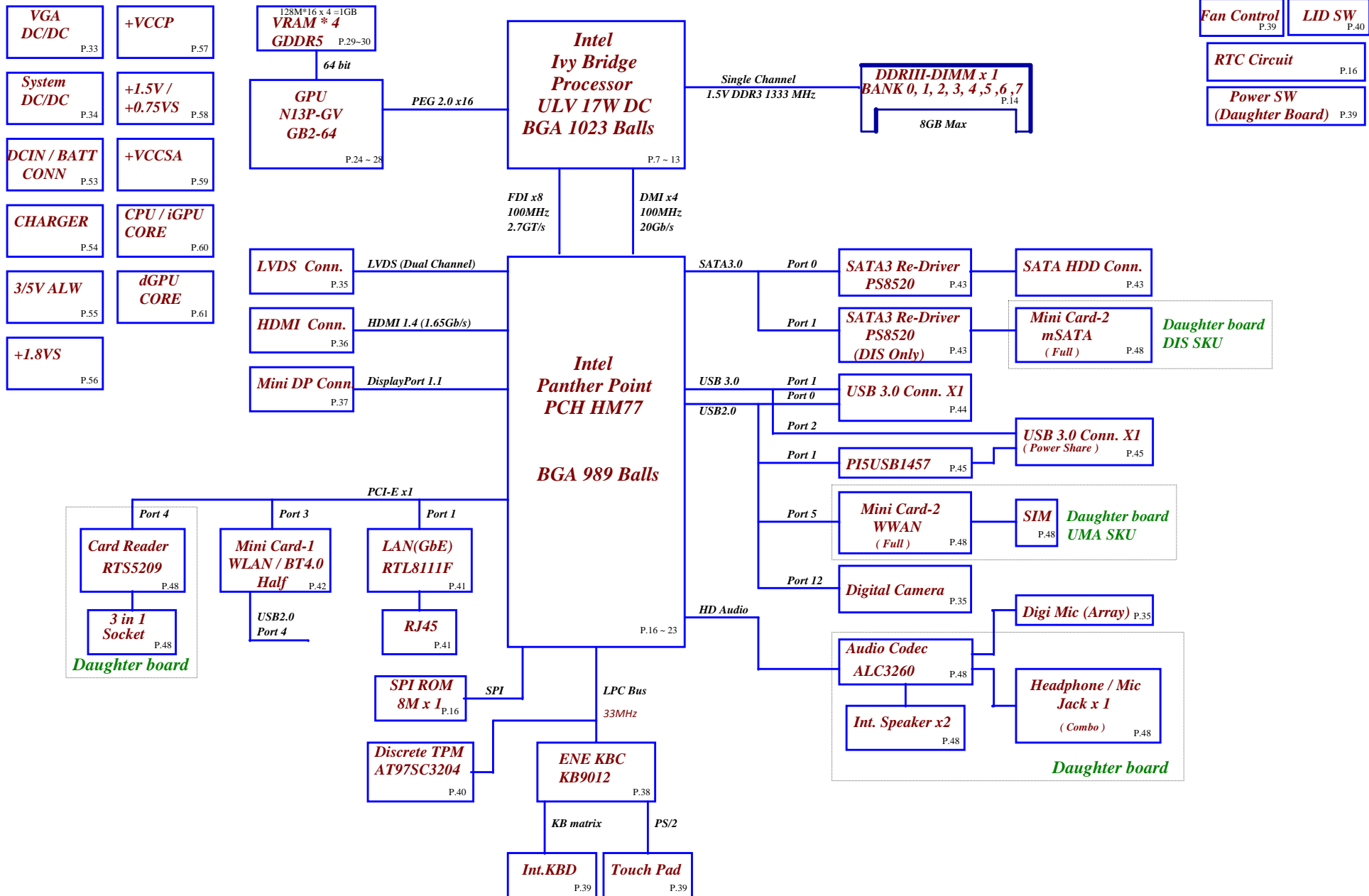
CONN@ : Connector Component

DIS@ : pop when DIS configuration

UMA@ : pop when UMA configuration

MB Type	BOM P/N	
TPM	4319EJ31L01	
TCM	4319EJ31L02	2@ 4@
TPM DIS/ TCM DIS		2@ 3@

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Cover Page
				Size Document Number
				LA-7841P
				Rev 0.3
				Date: Tuesday, February 07, 2012 Sheet 1 of 65



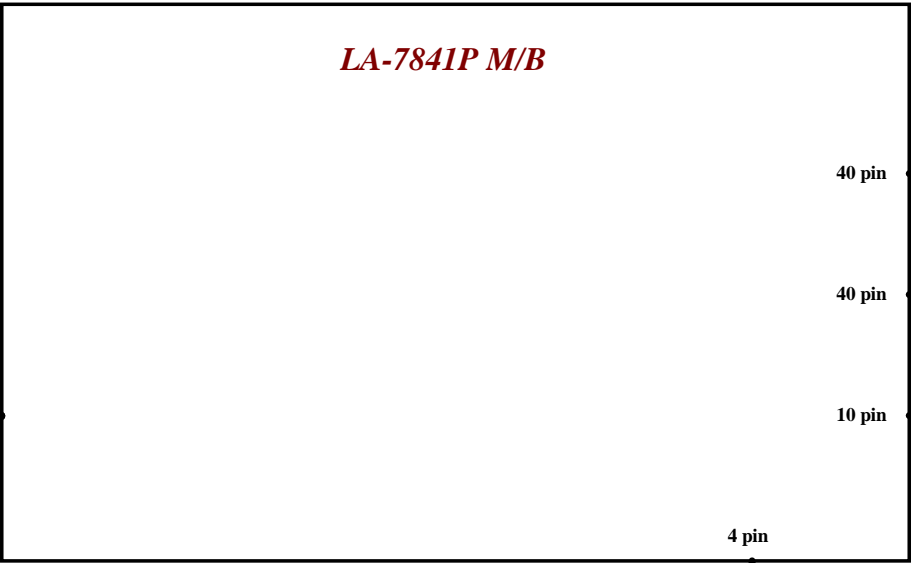
Compal Confidential

Project Code : QLM00
File Name : LA-7841P

LS-7841P POWER BUTTON BOARD
LS-7842P LED INDICATE BOARD
LS-7843P BATTERY INDICATED BOARD
LS-7844P I/O BOARD



Wire
6 pin



40 pin

Wire

Camera

LCD Panel

40 pin

FFC

IO/B

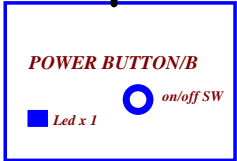
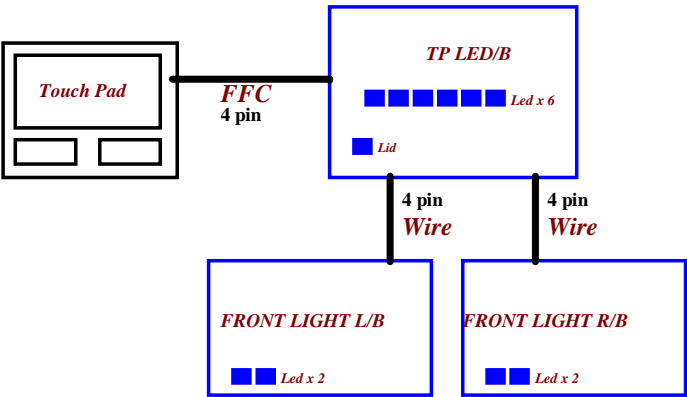
10 pin

Wire

HDD

4 pin

FFC



Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	Block Diagram	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev	0.3
				Date	Tuesday, February 07, 2012	Sheet 3 of 65

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Thermal Sensor 1	Thermal Sensor 2	FFS	VGA Thermal Sensor	VGA	DMC	XDPA	Charger
EC_SMB_CK1 EC_SMB_DA1	KB930			V									
EC_SMB_CK2 EC_SMB_DA2	KB930					V	V		V				
PCH_SML0CLK PCH_SML0DATA	PCH												
PCH_SML1CLK PCH_SML1DATA	PCH												V
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V			V		V	V	V	

Link

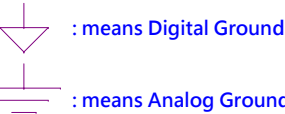
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	HDD
SATA1	None
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

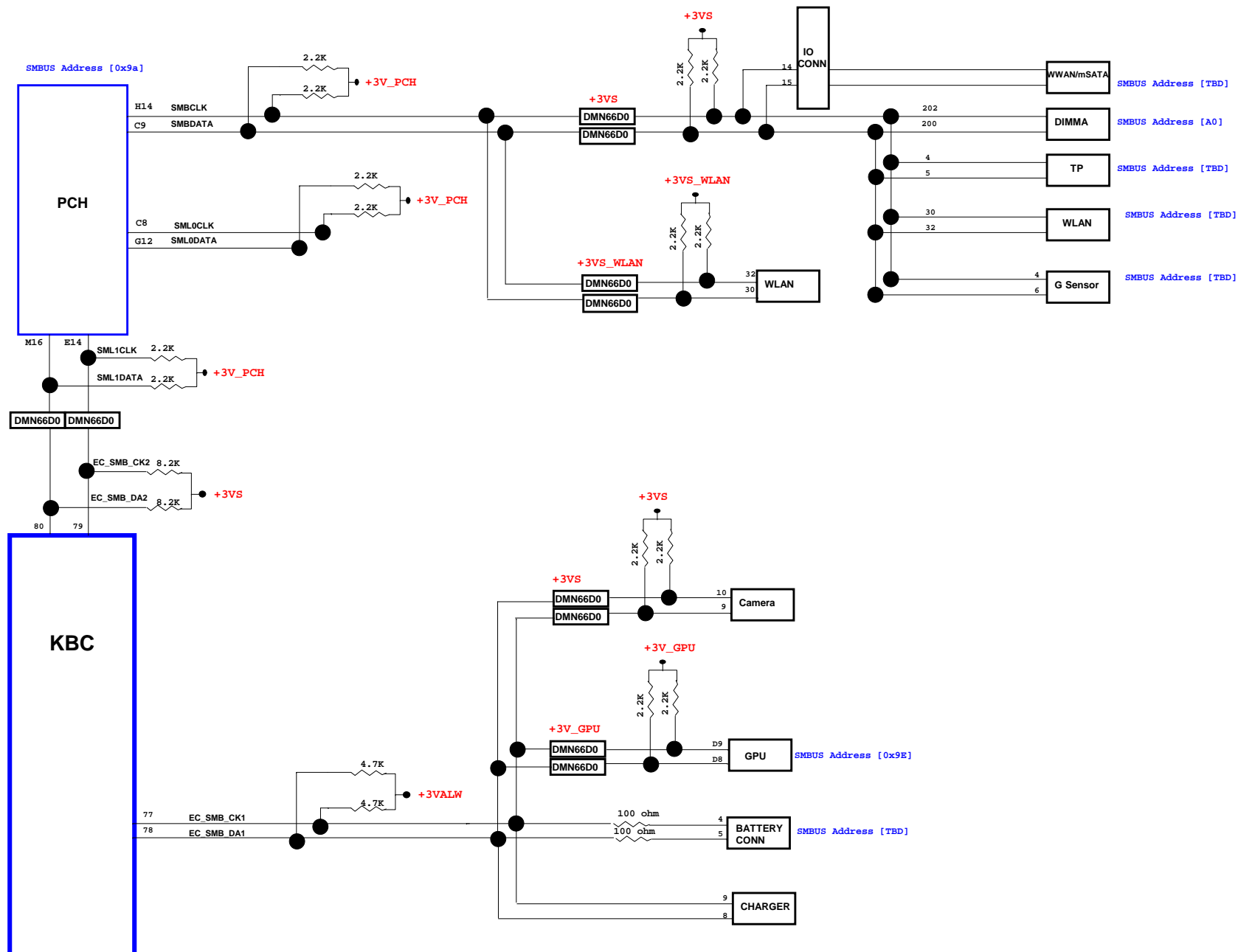
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-2 WWAN/DMC
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	USB 3.0
Lane 7	None
Lane 8	None

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	MINI CARD-2 WWAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	USB 3.0		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

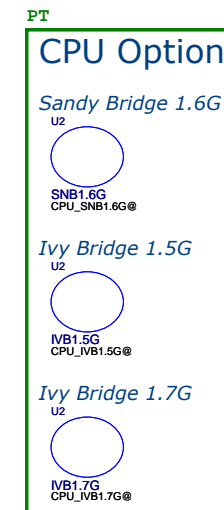
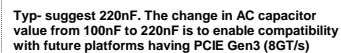
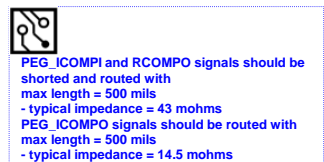
Symbol Note :



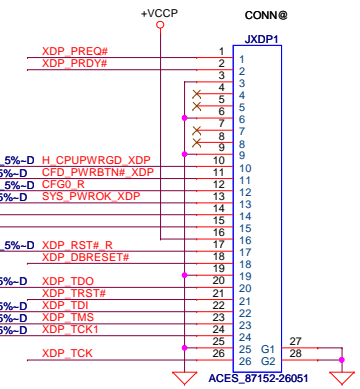
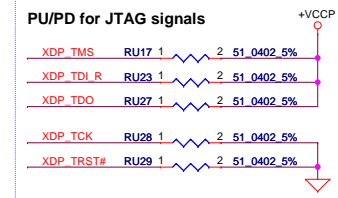
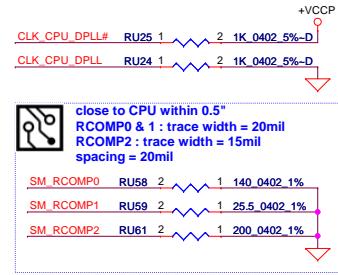
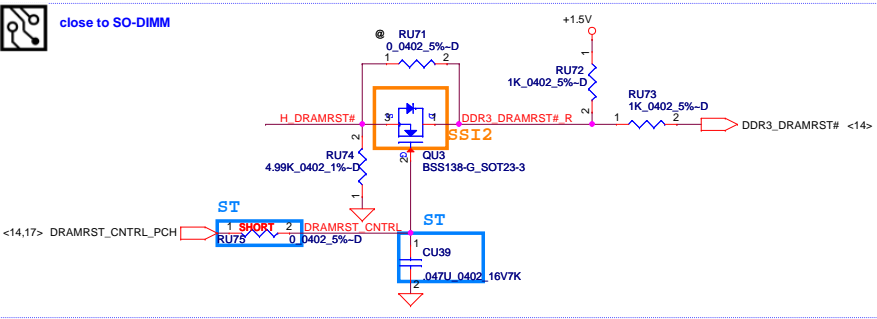
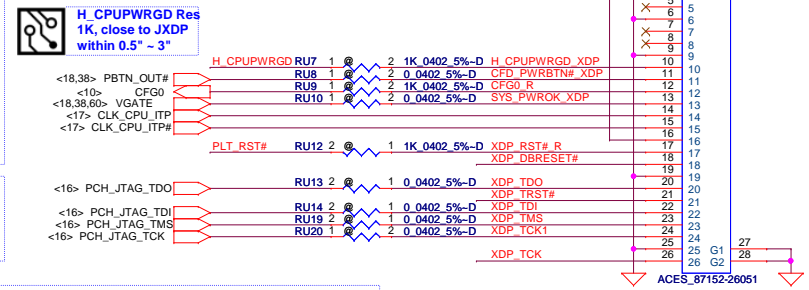
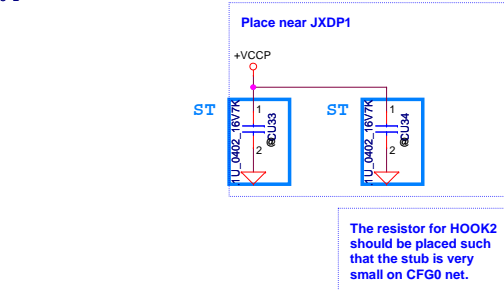
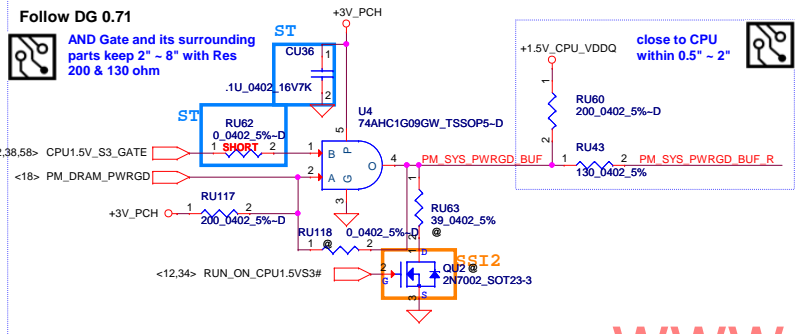
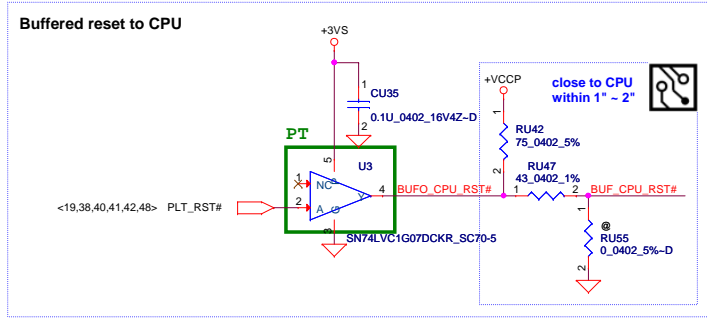
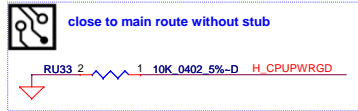
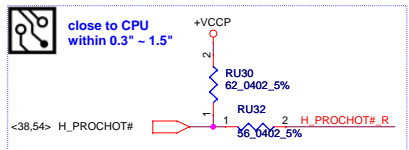
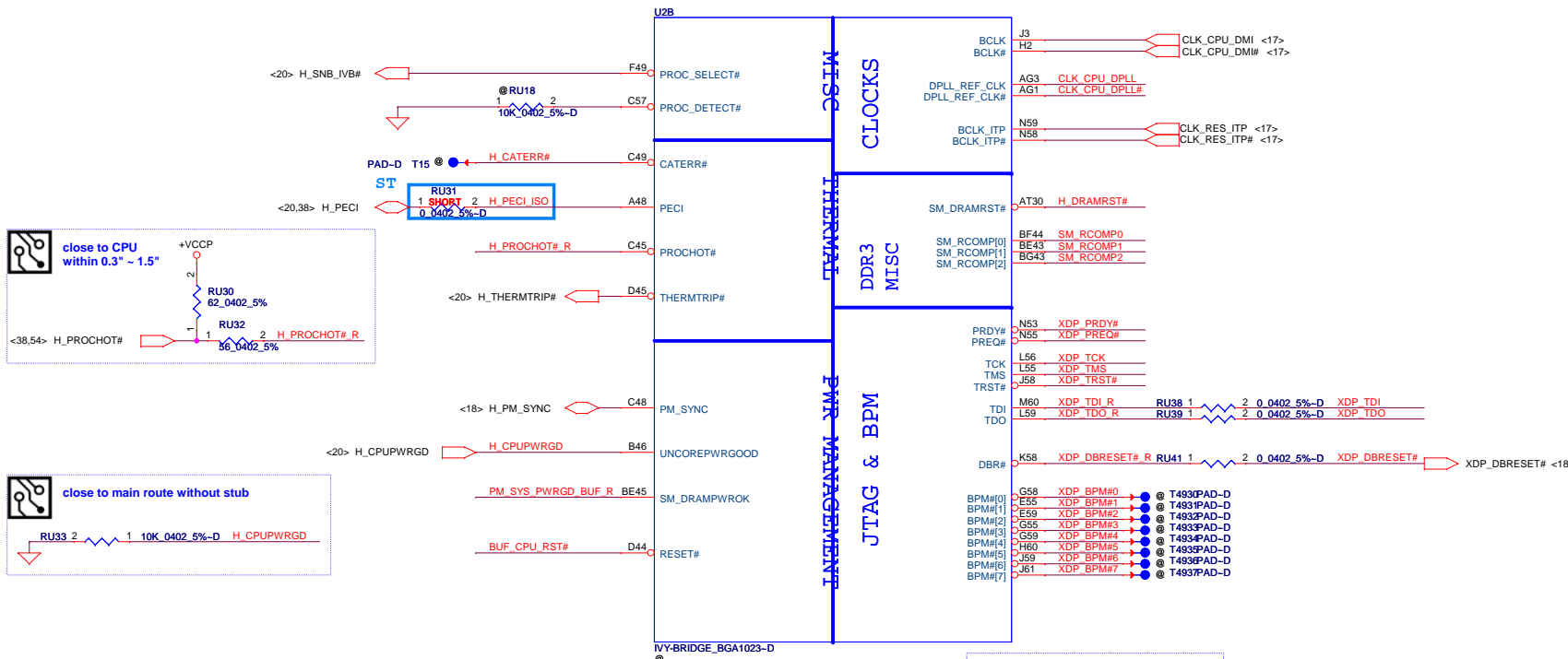
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Notes List
				Document Number
				LA-7841P
				Rev
				0.3
				Date
				Tuesday, February 07, 2012
				Sheet
				4
				of
				65



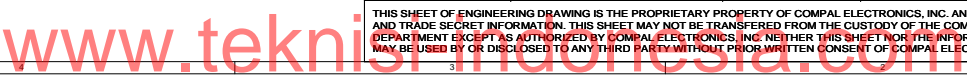
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	PROCESSOR(1/7) DML,FDI,PEG
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN PERMISSION OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Docu- ment Number	Rev 0.3
				Custom	
Date:				Tuesday, February 07, 2012	Sheet 5 of 65

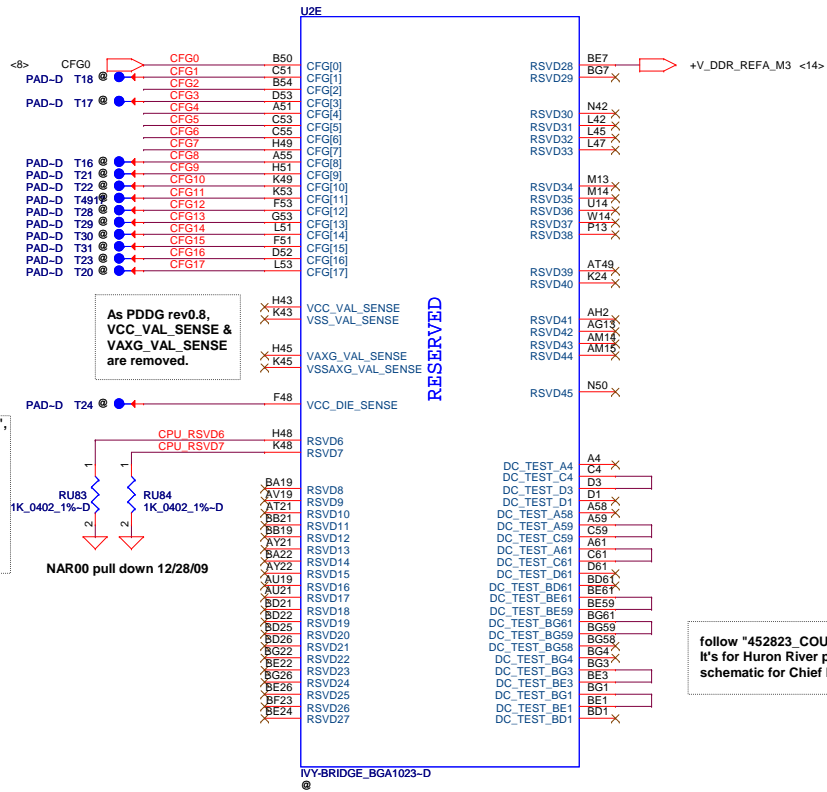


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		2011/07/15		Deciphered Date	
		2012/07/15		Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT TO ANY OTHER DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR(1/7) DMI,FDI,PEG	
				Document Number	
				Rev 0.3	
Date		Tuesday, February 07, 2012		Sheet 7 of 65	

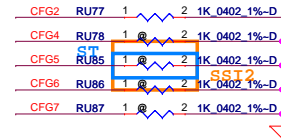


Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR(2/7) PM,XDP,CLK	
				Document Number	Rev
				Customer	0.3
				Date: Tuesday, February 07, 2012	Sheet 8 of 65





CFG Straps for Processor



		1 (Default value)	0
PCI Express* Static x16 Lane Numbering Reversal	CFG2	Normal operation (match socket pin map)	Lane numbers reversed
PCI Express* Static x4 Lane Numbering Reversal	CFG3	Normal operation (match socket pin map)	Lane numbers reversed
eDP enable	CFG4	Disable	Enable
PEG DEFER TRAINING	CFG7	PEG Train immediately following RESETB de-assertion	PEG Wait for BIOS for training

PCI Express Bifurcation (x16 Lane)	CFG[6:5]	11	1 x16 PCI Express (Default value)
		10	2 x8 PCI Express
		01	reserved
		00	1 x8, 2 x4 PCI Express

follow "452823_COUGAR_CANYON(BGA1023)_Customer_Ready_Schematic". It's for Huron River platform, since can't find CPU Ivy bridge BGA1023 schematic for Chief River at this moment.

+VCC_CORE decoupling
Cap. in Page 62.

ULV 17W, Max Current
in Turbo Mode or HFM

POWER

+VCCP decoupling
Cap. in Page 62.

+VCCP
8.5A

CORE SUPPLY

PEG IO AND DDR IO

QUIET
RAILS

SVZD

SENSE LINES

- A26 VCC[1]
- A39 VCC[2]
- A31 VCC[3]
- A34 VCC[4]
- A35 VCC[5]
- A38 VCC[6]
- A39 VCC[7]
- A42 VCC[8]
- C26 VCC[9]
- C27 VCC[10]
- C32 VCC[11]
- C34 VCC[12]
- C37 VCC[13]
- C39 VCC[14]
- C42 VCC[15]
- D27 VCC[16]
- D32 VCC[17]
- D34 VCC[18]
- D37 VCC[19]
- D39 VCC[20]
- D42 VCC[21]
- E26 VCC[22]
- E28 VCC[23]
- E32 VCC[24]
- E34 VCC[25]
- E37 VCC[26]
- E38 VCC[27]
- F25 VCC[28]
- F26 VCC[29]
- F28 VCC[30]
- F32 VCC[31]
- F34 VCC[32]
- F37 VCC[33]
- F38 VCC[34]
- F42 VCC[35]
- G42 VCC[36]
- H25 VCC[37]
- H26 VCC[38]
- H28 VCC[39]
- H29 VCC[40]
- H32 VCC[41]
- H34 VCC[42]
- H35 VCC[43]
- H37 VCC[44]
- H38 VCC[45]
- H40 VCC[46]
- J25 VCC[47]
- J28 VCC[48]
- J29 VCC[49]
- J32 VCC[50]
- J34 VCC[51]
- J35 VCC[52]
- J37 VCC[53]
- J38 VCC[54]
- J40 VCC[55]
- J42 VCC[56]
- K26 VCC[57]
- K27 VCC[58]
- K29 VCC[59]
- K32 VCC[60]
- K34 VCC[61]
- K35 VCC[62]
- K37 VCC[63]
- K42 VCC[64]
- L25 VCC[65]
- L28 VCC[66]
- L33 VCC[67]
- L36 VCC[68]
- L40 VCC[69]
- N26 VCC[70]
- N30 VCC[71]
- N34 VCC[72]
- N38 VCC[73]
- N39 VCC[74]
- N42 VCC[75]
- N44 VCC[76]

- VCCIO[1] AF46
- VCCIO[3] AG48
- VCCIO[4] AG50
- VCCIO[5] AG51
- VCCIO[6] AJ17
- VCCIO[7] AJ21
- VCCIO[8] AJ25
- VCCIO[9] AJ43
- VCCIO[10] AJ47
- VCCIO[11] AK50
- VCCIO[12] AK51
- VCCIO[13] AL14
- VCCIO[14] AL15
- VCCIO[15] AL16
- VCCIO[16] AL20
- VCCIO[17] AL22
- VCCIO[18] AL26
- VCCIO[19] AL45
- VCCIO[20] AL48
- VCCIO[21] AM16
- VCCIO[22] AM17
- VCCIO[23] AM21
- VCCIO[24] AM43
- VCCIO[25] AM47
- VCCIO[26] AN20
- VCCIO[27] AN42
- VCCIO[28] AN45
- VCCIO[29] AN48
- VCCIO[30] AA14
- VCCIO[31] AA15
- VCCIO[32] AB17
- VCCIO[33] AB20
- VCCIO[34] AC13
- VCCIO[35] AD16
- VCCIO[36] AD18
- VCCIO[37] AD21
- VCCIO[38] AE14
- VCCIO[39] AE15
- VCCIO[40] AF16
- VCCIO[41] AF18
- VCCIO[42] AF20
- VCCIO[43] AG15
- VCCIO[44] AG16
- VCCIO[45] AG17
- VCCIO[46] AG20
- VCCIO[47] AG21
- VCCIO[48] AJ14
- VCCIO[49] AJ15

VCCIO50
VCCIO51

VCCIO_SEL

VCCPQE[1]
VCCPQE[2]

VIDALERT#
VIDSCLK
VIDSOUT

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSS_SENSE_VCCIO

+VCCP

BC22

+VCCP

A44
B43
C44

F43
G43

AN16
AN17

RU100
RU103

W16
W17

CU40

CU94

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1

2

1

2

1

2

1

2

1

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

CU94

1U_0402_6.3V6K-D

RU94

RU92

F43
G43

AN16
AN17

RU100
RU103

1

2

1

2

1

2

1

2

1

2

1

2

1U_0402_6.3V6K-D

T25 PAD-D

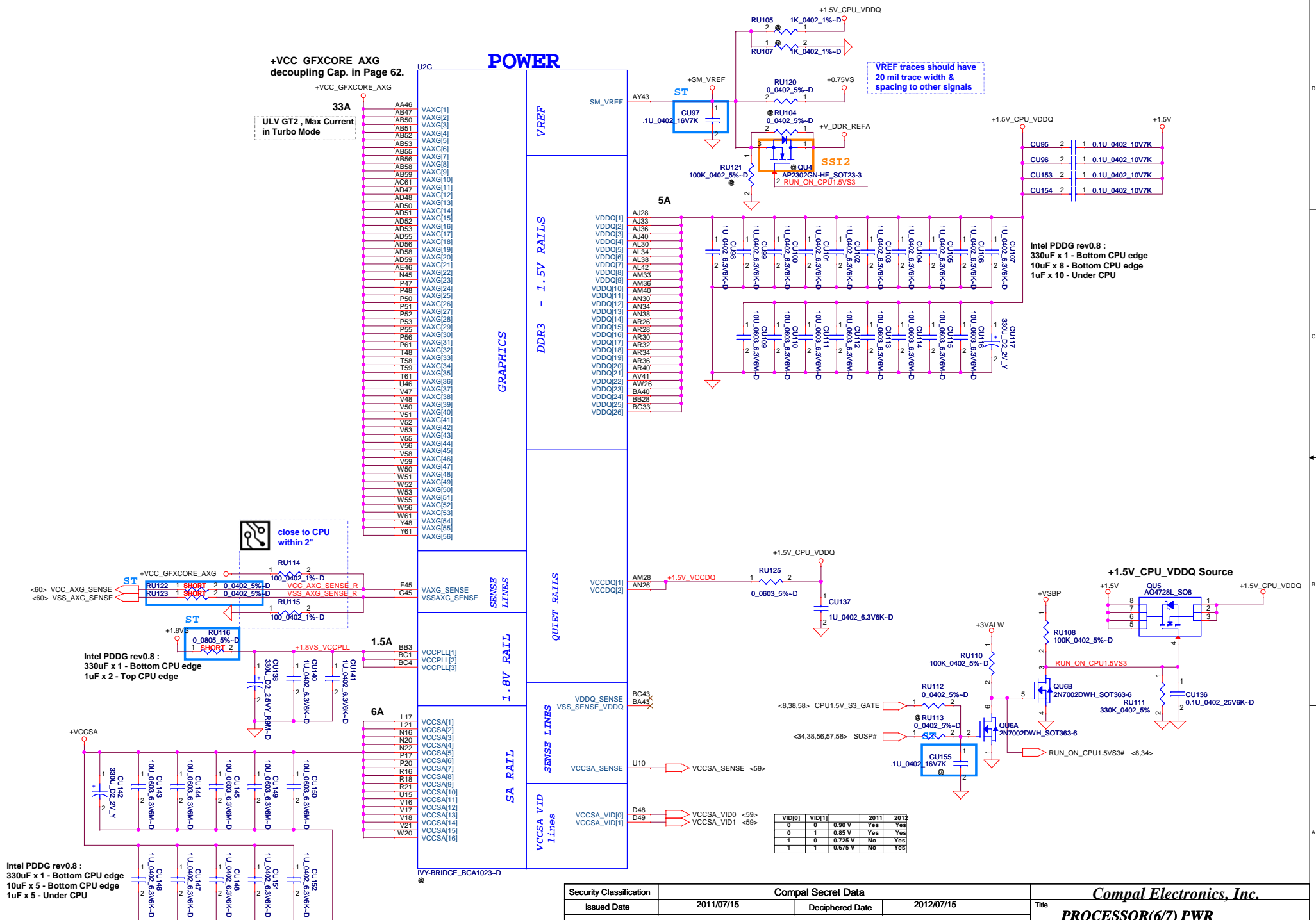
CU94

1U_0402_6.3V6K-D

RU94

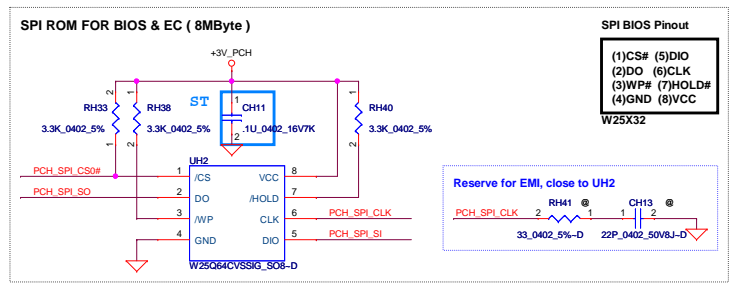
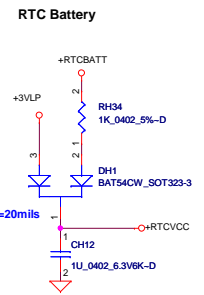
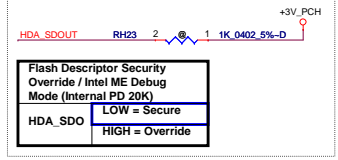
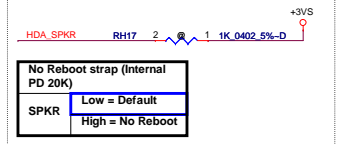
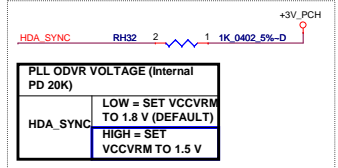
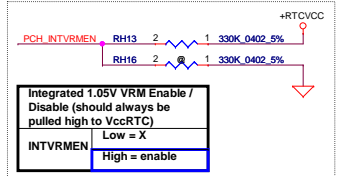
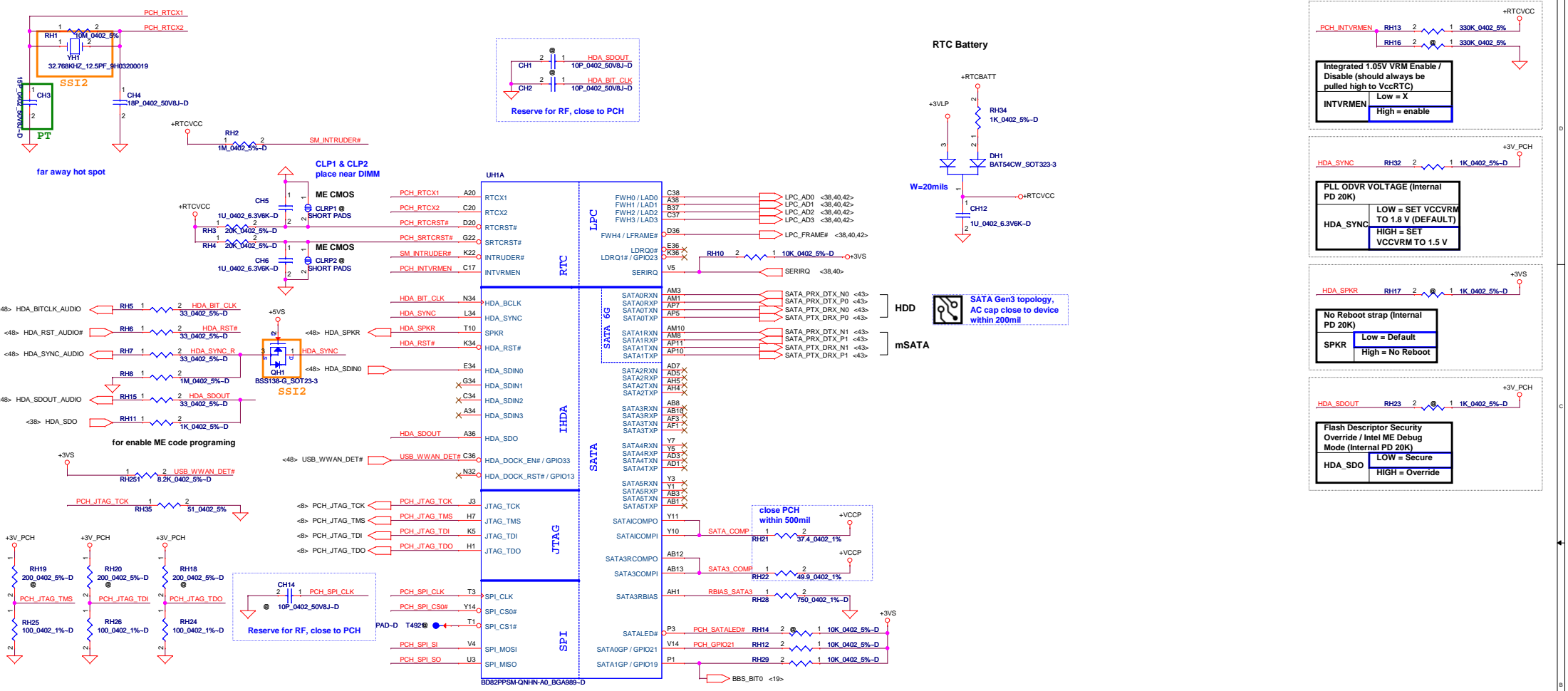
RU92

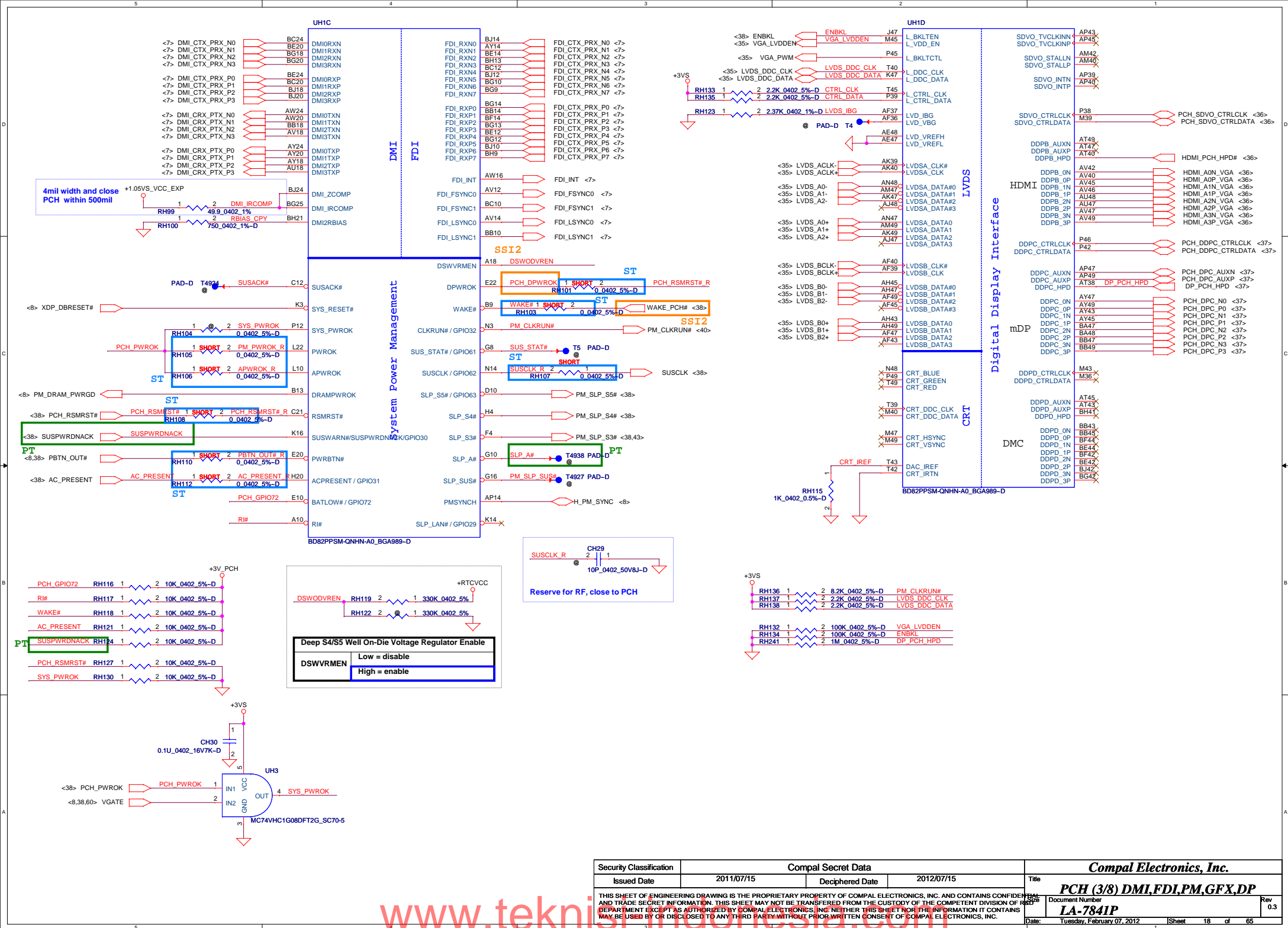
F43
G43

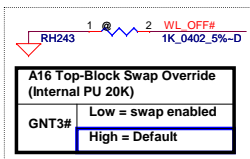


intent to blank

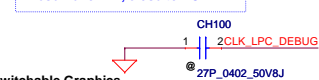
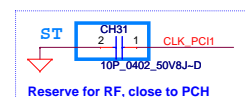
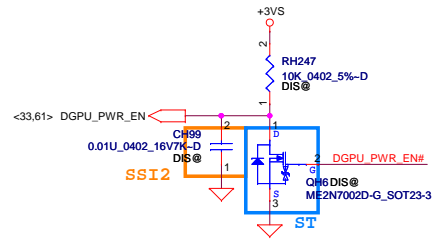
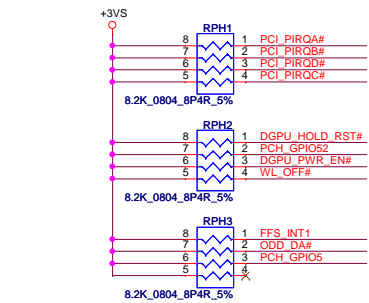
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	DDRIII DIMMB
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7841P	0.3
Date: Tuesday, February 07, 2012				Sheet	15 of 65



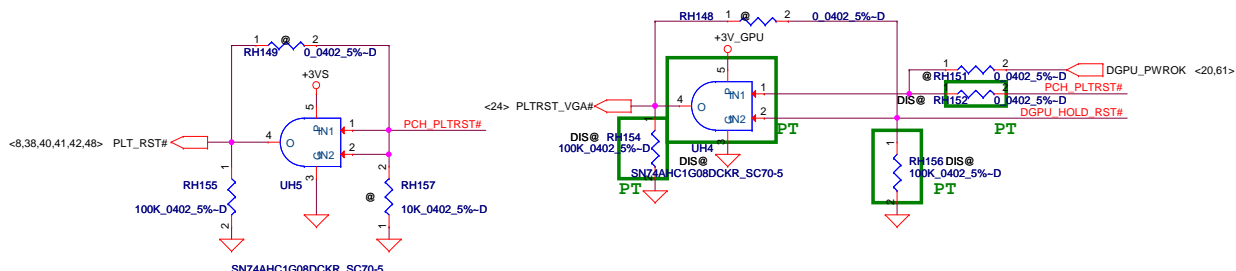
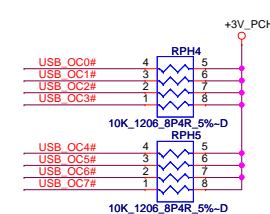
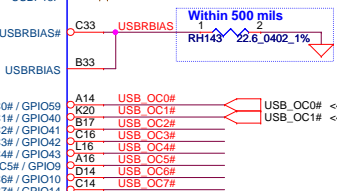
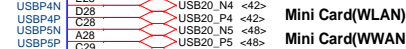
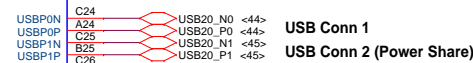
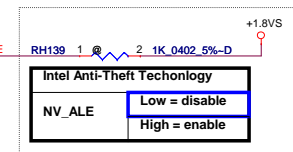
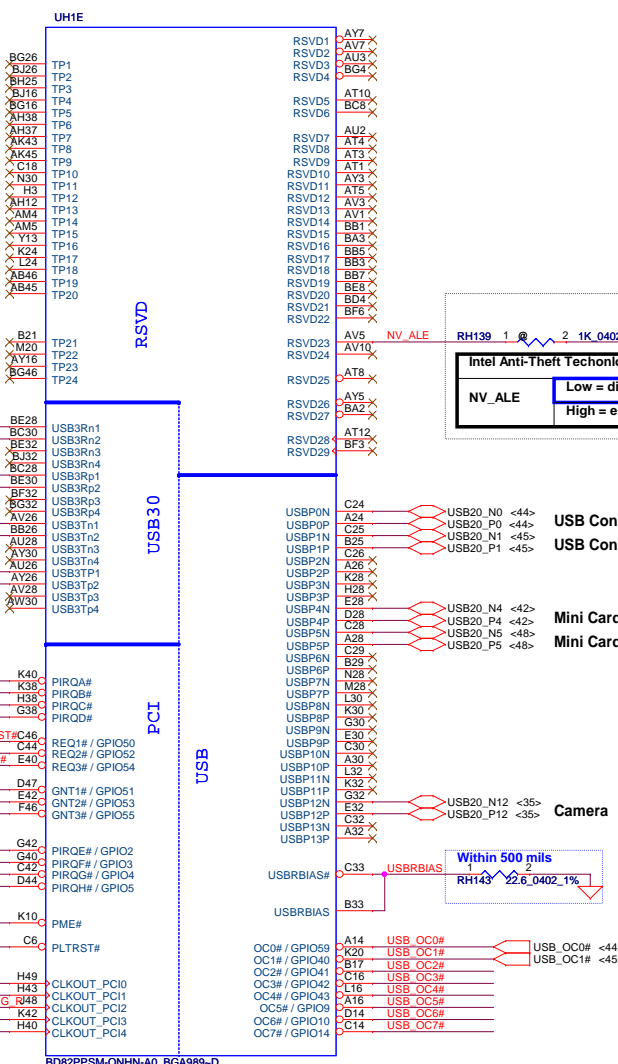
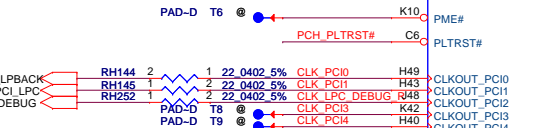
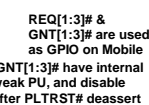
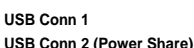




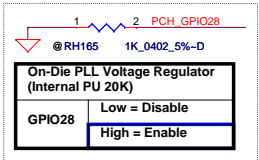
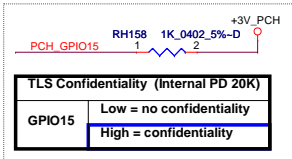
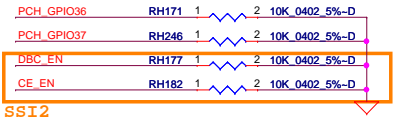
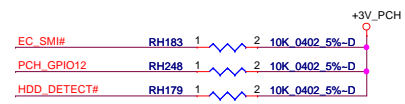
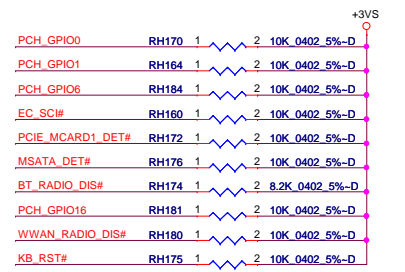
BIT 1	BIT 0	Boot BIOS Location
GNT1#	SATA1GP	
0	0	LPC
0	1	Reserved
1	0	PCI(non-mobile)
1	1	SPI



Switchable Graphics						
Signal	GPIO	Type	During Reset	After Reset	Usage	Description
DGPU_PWR_EN#	GPIO54	Output	High	High	Must have	Driven by Switchable Graphics Driver to turn on/off the discrete graphics power. 0 = dGPU power switch turned on 1 = Power switch turned off
DGPU_PWROK	GPIO17	Input	-	-	Must have	Driven by dGPU VR to indicate the power status to PCH. Used to enable clocks to dGPU. 0 = dGPU power is not stable. Keep clock disabled & reset asserted. 1 = dGPU power is stable. Clock can be enabled; reset can be deasserted If DGPU_PRSENT# is 1, in-order to get regular discrete GFX cards working, program DGPU_PWROK as GPIO and assert a high value (1) on the pin.
DGPU_HOLD_RST#	GPIO50	Output	Low	Low	Must have	Discrete Graphics Enable signal. Controlled by Switchable Graphics Driver and driven by PCH GPIO. Used to gate with Platform Reset to enable the Reset for dGPU. 0 = Keep dGPU in reset. 1 = Reset is released. This action taken 100 ms after DGPU_PWROK to ensure clock is stable.

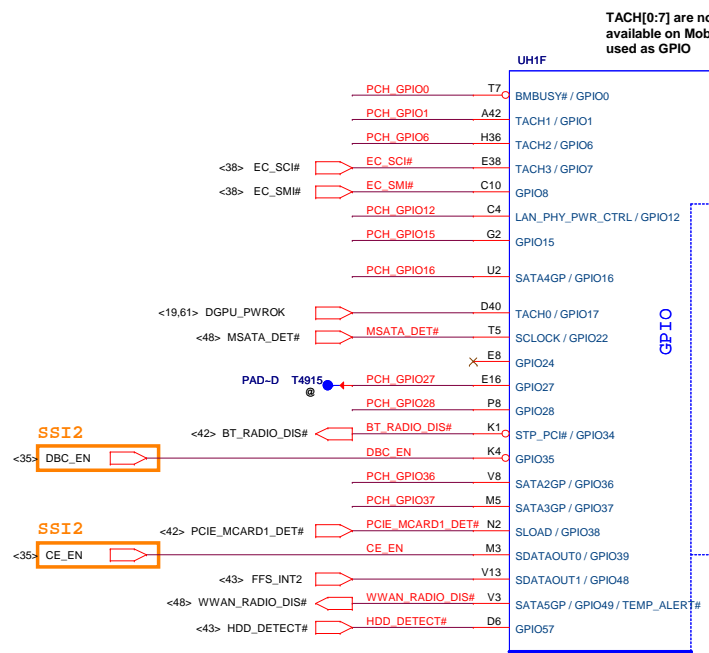


Security Classification	Compal Secret Data			Compal Electronics, Inc. PCH (4/8) PCI, USB, NVRAM		
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT TO ANY OTHER DEPARTMENT OR DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.3	
				LA-7841P Date: Tuesday, February 07, 2012	Sheet 19 of 65	



PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

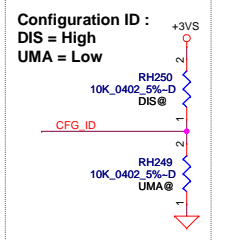
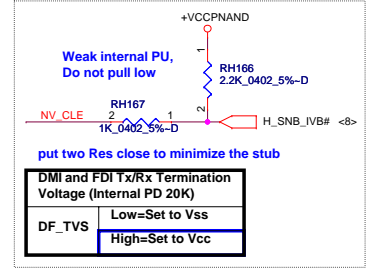
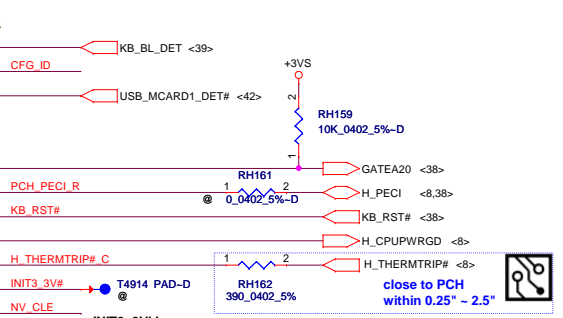
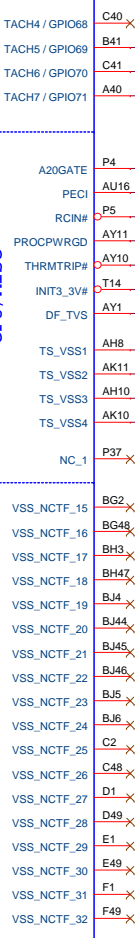
Please refer to Huron River Debug Board DG 0.5

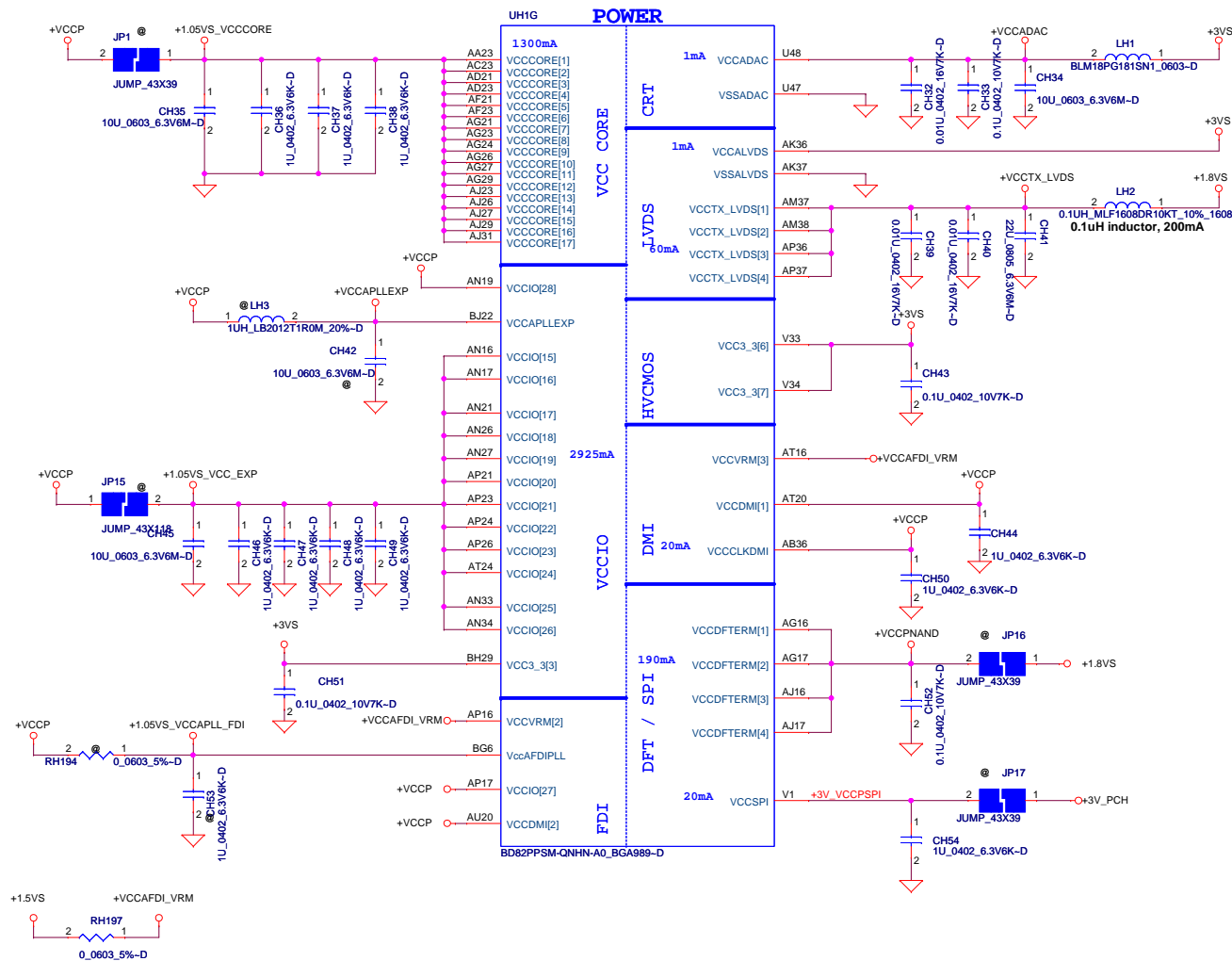


TACH[0:7] are not available on Mobile, used as GPIO

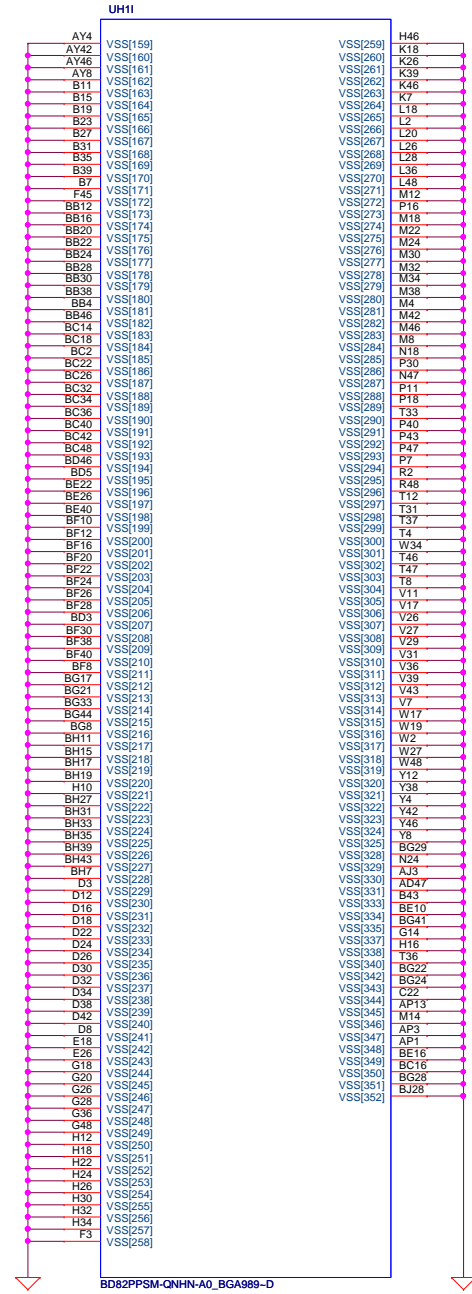
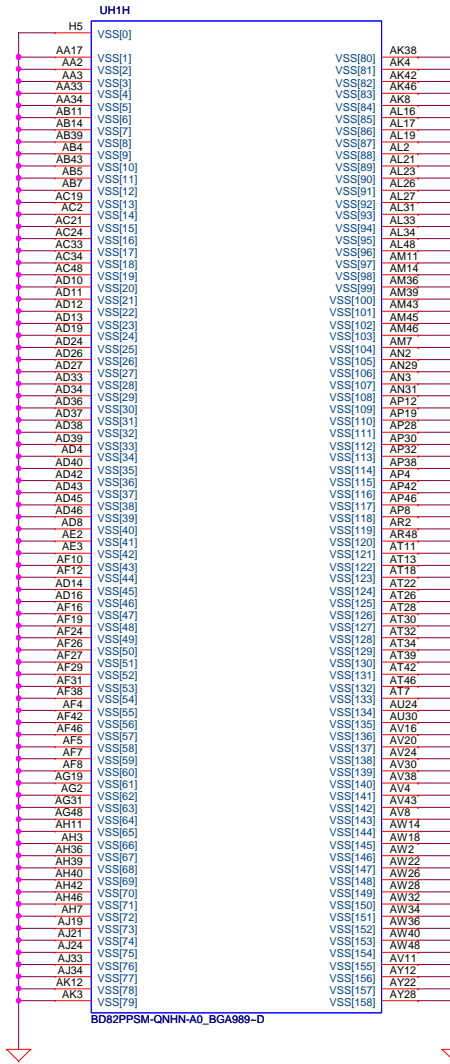
CPU/MISC

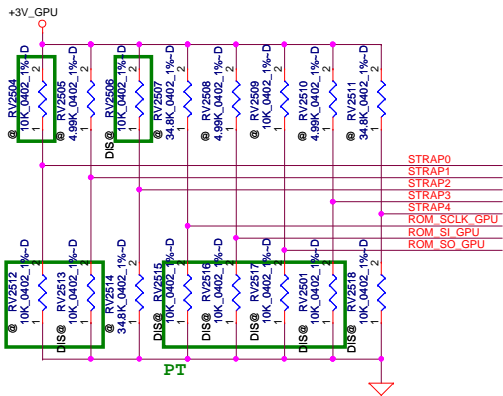
NCTF





Voltage Rail	Voltage	60 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



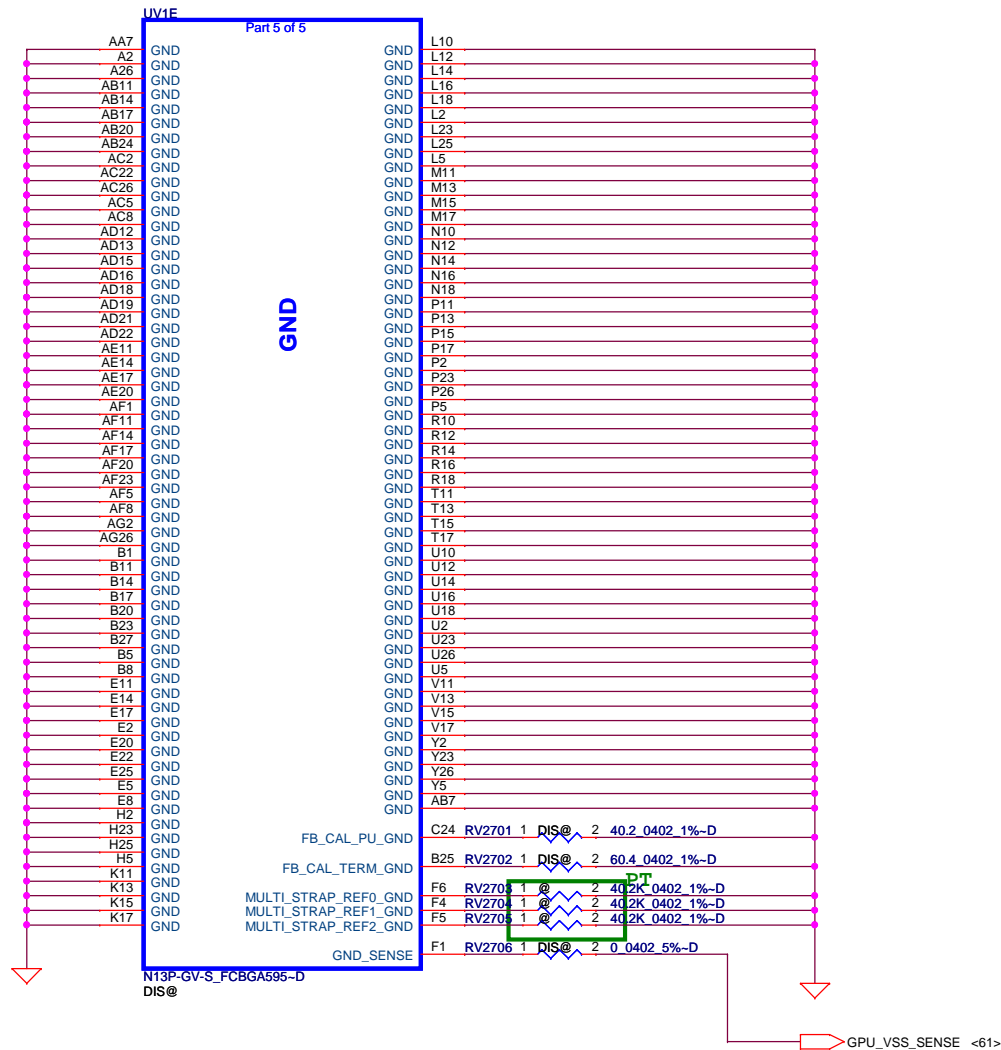


Vendor	STRAP[3:0]
Samsung 128MX16 (SA000048E0L)	0 1 0 1
Hynix 128MX16 (SA00004GD0L)	0 1 0 0

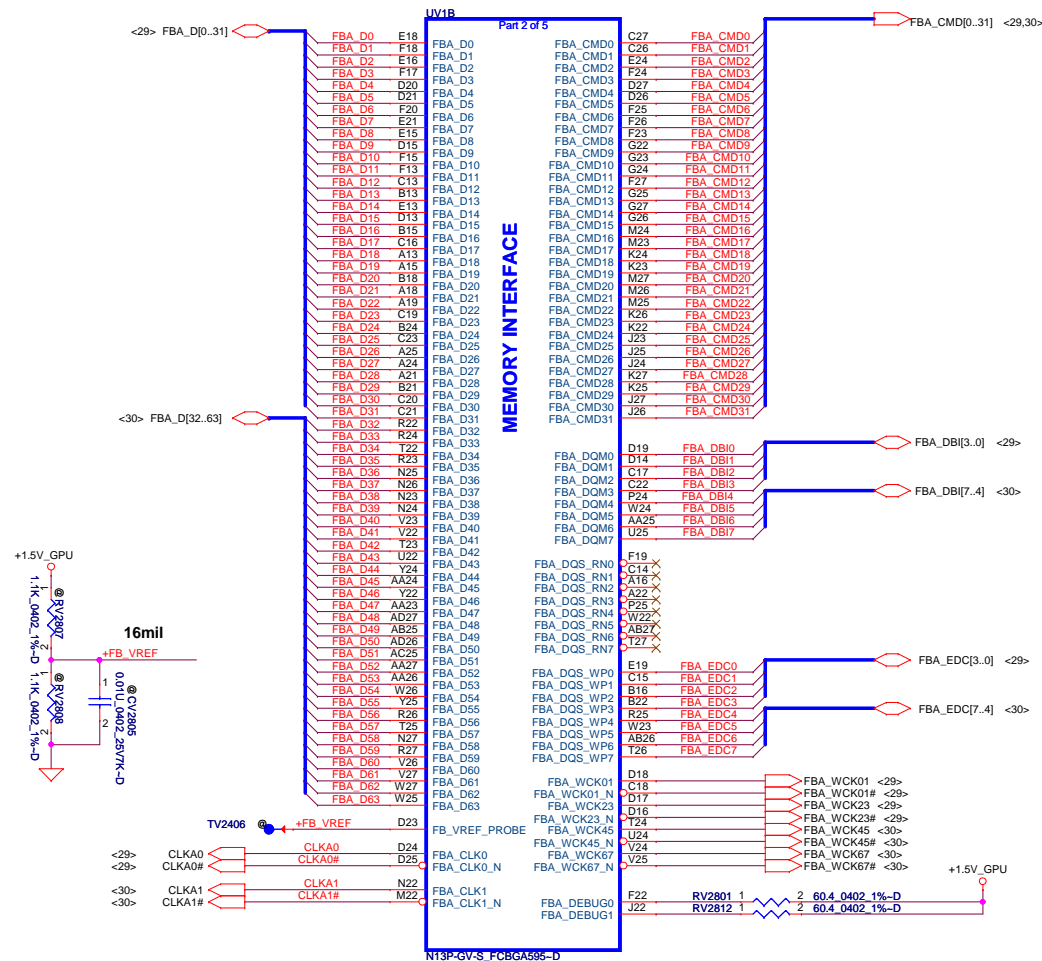
N13P-GV-S-A2	0x1140
--------------	--------

Binary Mode Straps

STRAP Pin Name	STRAP Mapping	Resistance	Polarity
STRAP0	RAM_CFG[0]	10K Ohm	For Hynix Pull-down 10K ohm to GND, Samsung pull-high 10K ohm to 3.3V
STRAP1	RAM_CFG[1]	10K Ohm	Pull-down 10K ohm to GND
STRAP2	RAM_CFG[2]	10K Ohm	Pull-up 10K ohm to +3V_GPU
STRAP3	RAM_CFG[3]	10K Ohm	Pull-down 10K ohm to GND
STRAP4	PCIE_MAX_SPEED	10K Ohm	Pull-down 10K ohm to GND
ROM_SCLK	SMB_ALT_ADDR	10K Ohm	Pull-down 10K ohm to GND
ROM_SI	SUB_VENDOR	10K Ohm	Pull-down 10K ohm to GND
ROM_SO	VGA_DEVICE	10K Ohm	Pull-down 10K ohm to GND



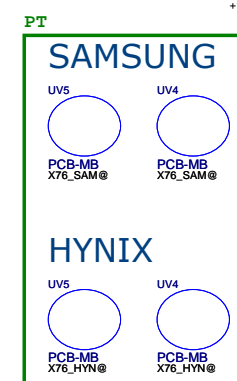
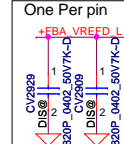
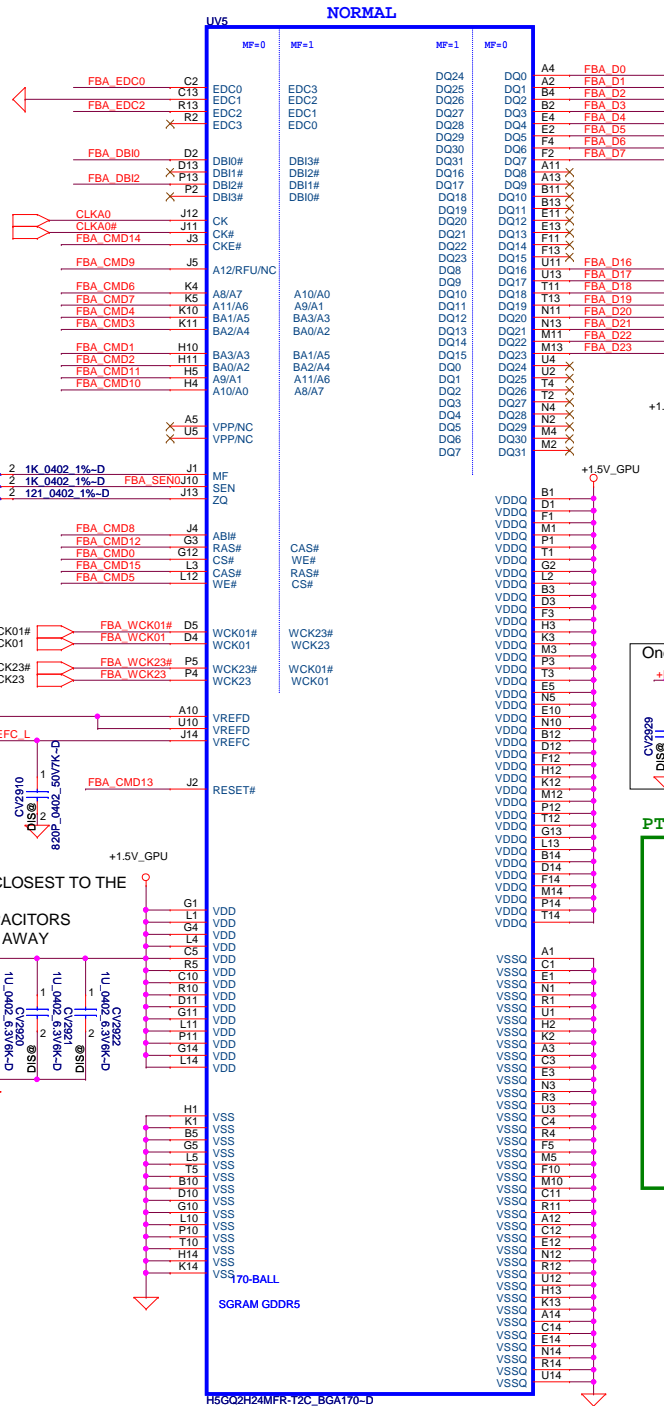
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	N13P(4/5) GND
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7841P
				Date:	Tuesday, February 07, 2012
				Sheet	27 of 65



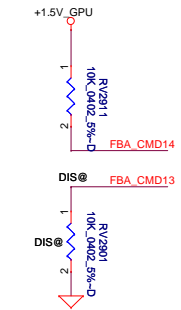
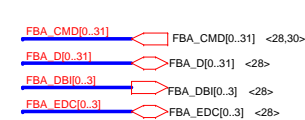
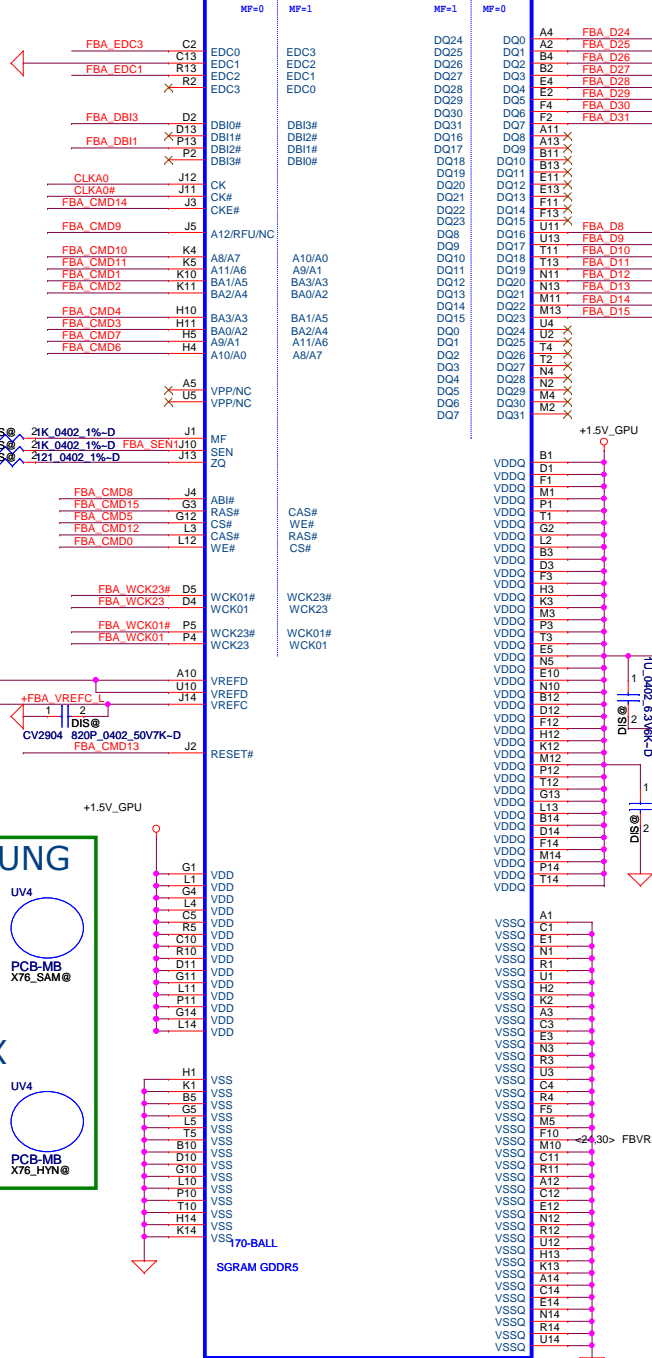
Mode H - Command Mapping

DATA Bus		
Address	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS#	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*

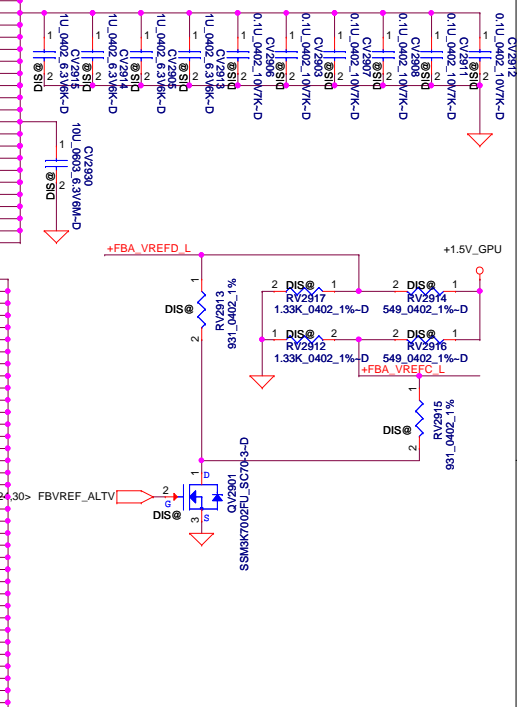
GDDR5 Mode H Mapping	
GB2-64	Channel 0 0...31
CMD0	CS#
CMD1	A3_BA3
CMD2	A2_BA0
CMD3	A4_BA2
CMD4	A5_BA1
CMD5	WE#
CMD6	A7_A8
CMD7	A6_A11
CMD8	AB1#
CMD9	A12_RFU
CMD10	A0_A10
CMD11	A1_A9
CMD12	RAS#
CMD13	RST#
CMD14	CKE#
CMD15	CA#



PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



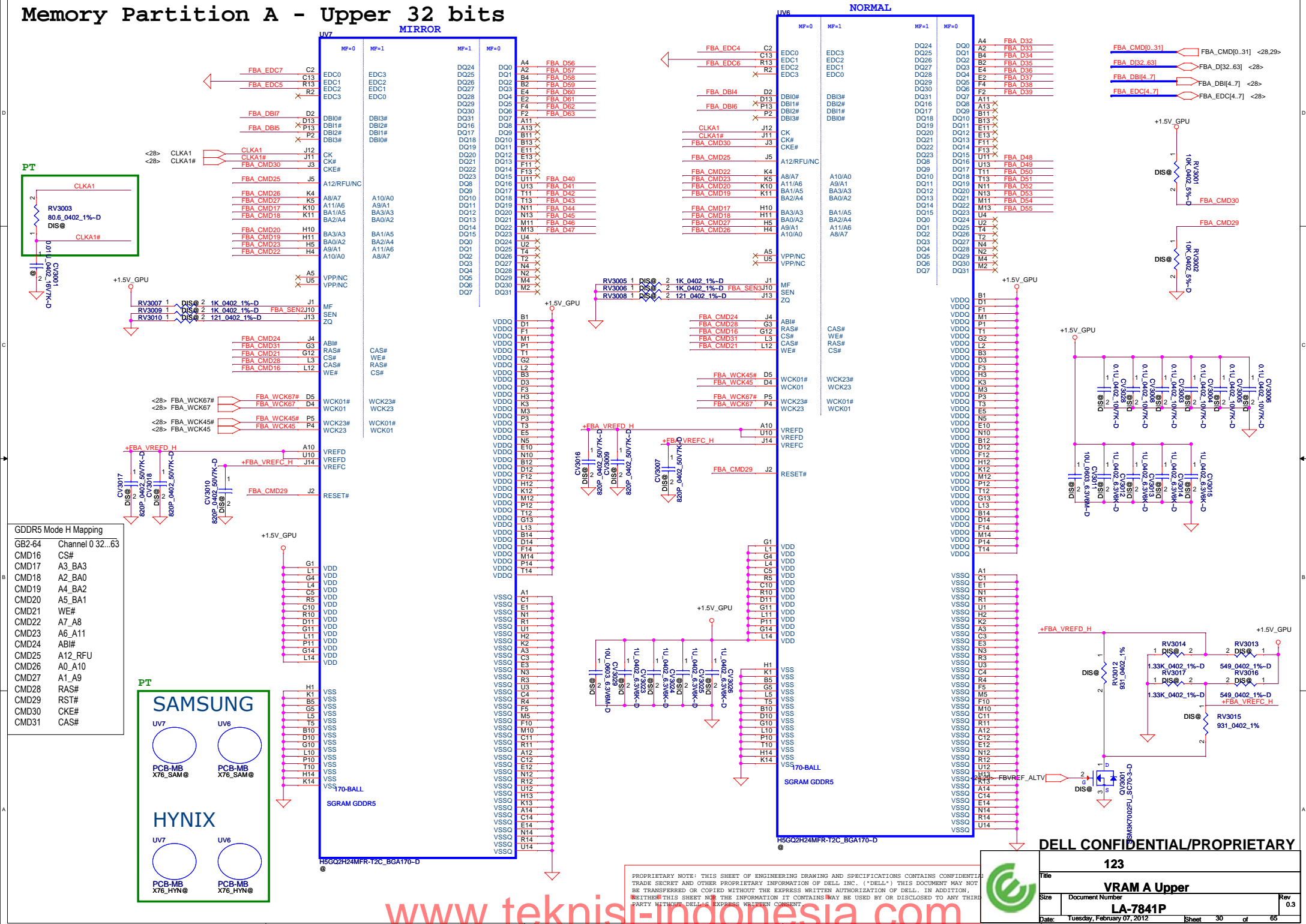
PLACE 0.1uF CAPS CLOSEST TO THE
MEMORY DEVICES
PLACE LARGER CAPACITORS
SLIGHTLY FARTHER AWAY



DELL CONFIDENTIAL/PROPRIETARY

123			
Title			
VRAM A Lower			
Size	Document Number		Rev
	LA-7841P		0.3
Date:	Tuesday, February 07, 2012	Sheet	29 of 65

Memory Partition A - Upper 32 bits



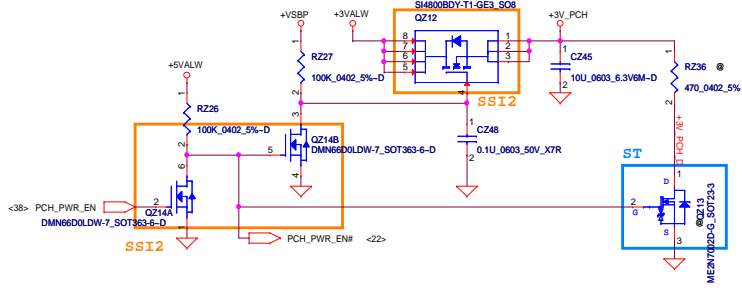
intent to blank

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.3
Date: Tuesday, February 07, 2012				Sheet 31	of 65

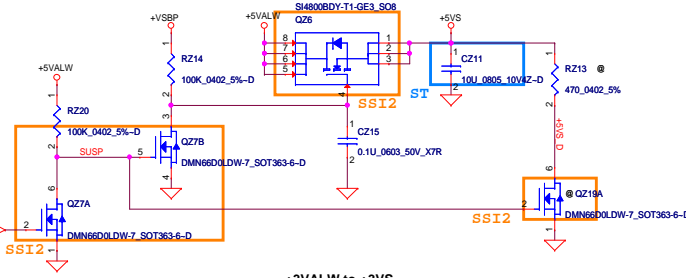
intent to blank

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.3
Date: Tuesday, February 07, 2012				Sheet 32 of 65	1

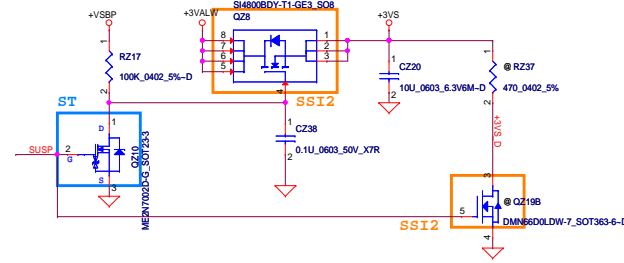
+3VALW to +3V_PCH



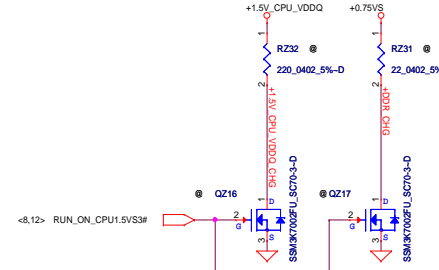
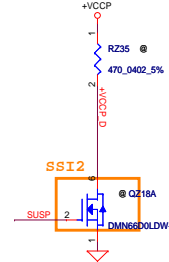
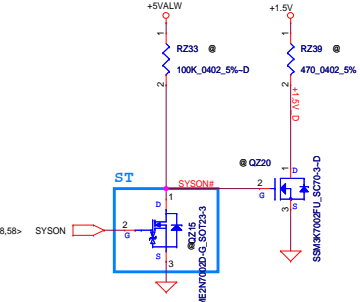
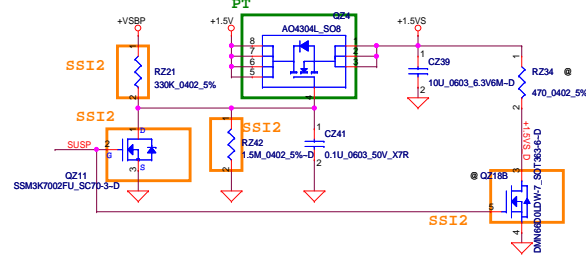
+5VALW to +5VS



+3VALW to +3VS

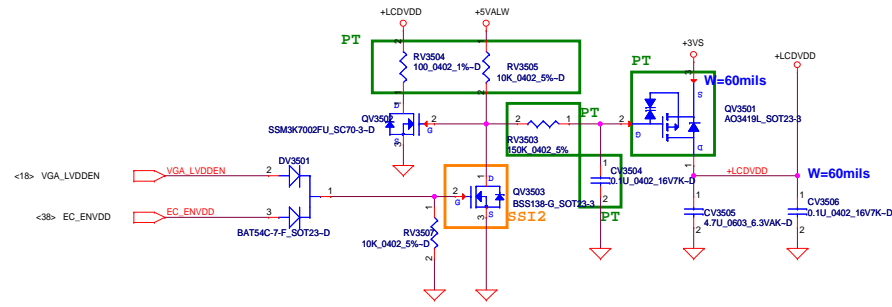


+1.5V To +1.5VS

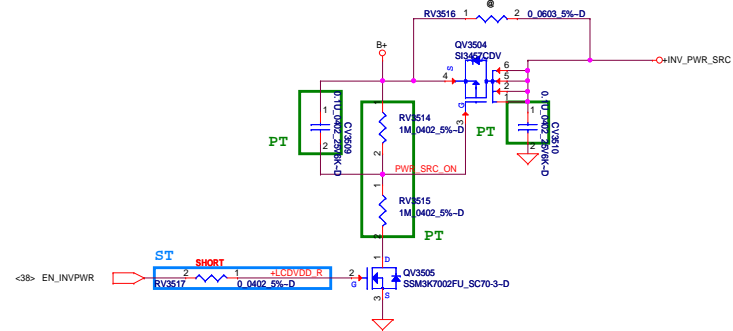


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				DC/DC Interface
LA-7841P				Rev 0.3
Date: Tuesday, February 07, 2012				Sheet 34 of 65

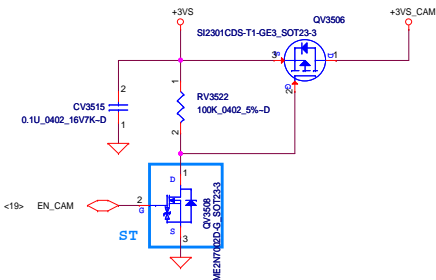
LCD PWR CTRL



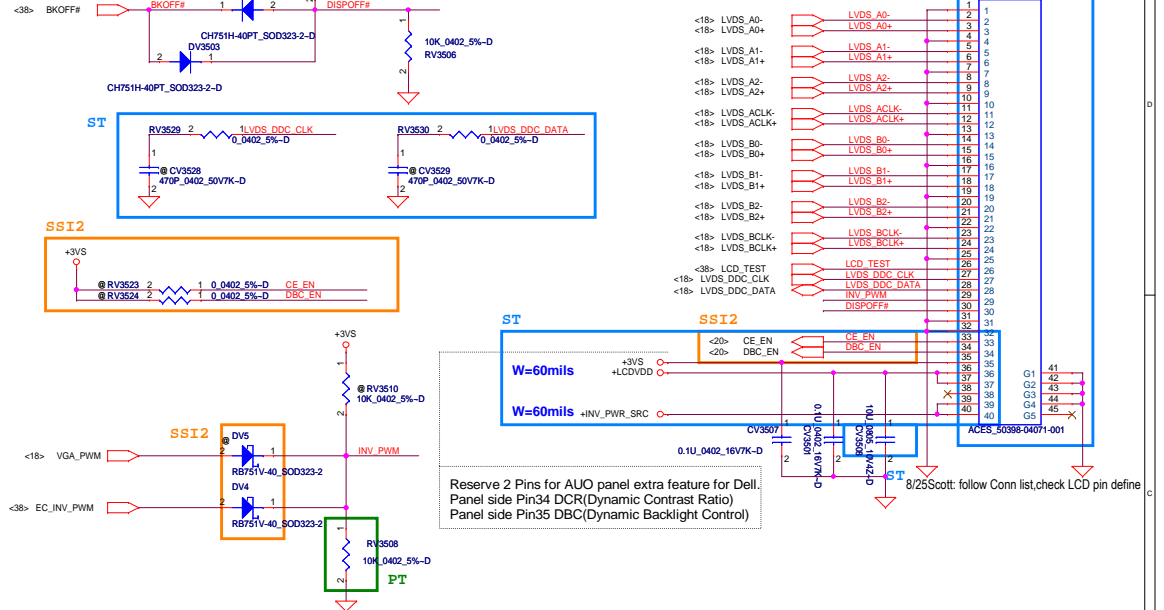
LCD backlight PWR CTRL



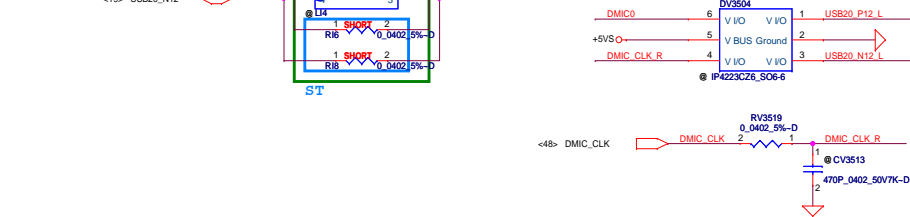
Webcam PWR CTRL



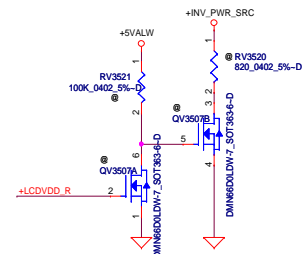
LVDS Conn.



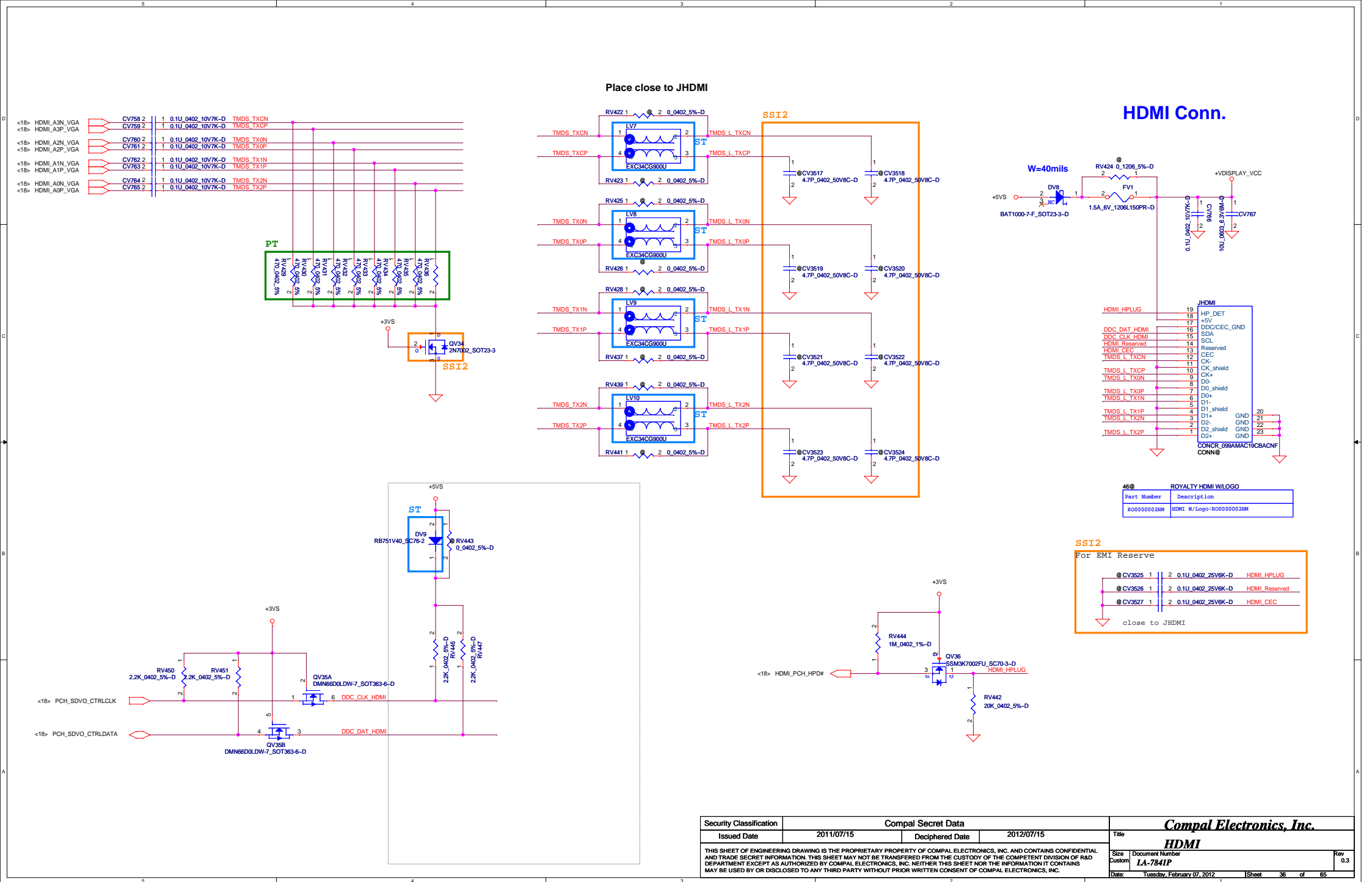
Webcam Conn.

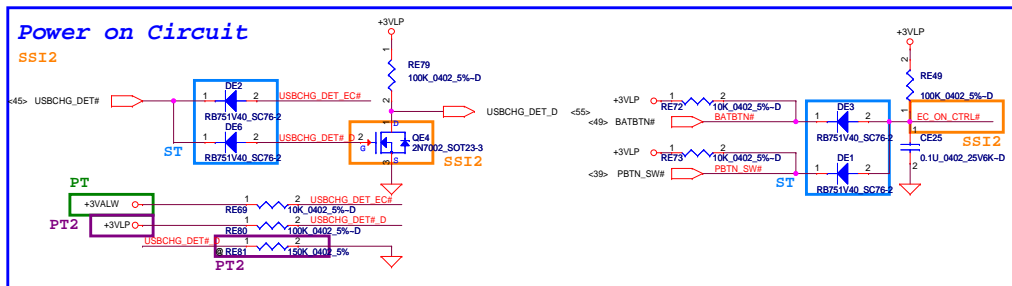
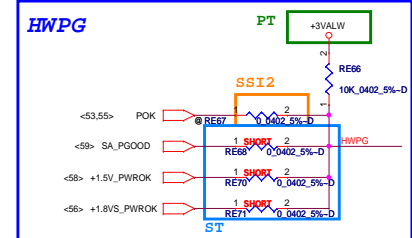


*** Reserved for LCD sequence tuning**



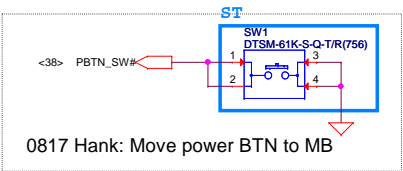
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number
				LA-7841P
				Rev 0.3
				Date: Tuesday, February 07, 2012
				Sheet 35 of 65



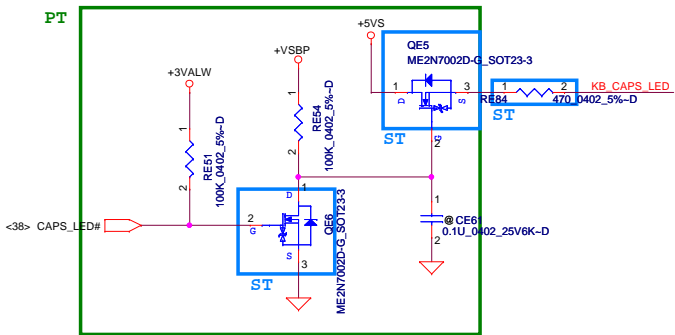
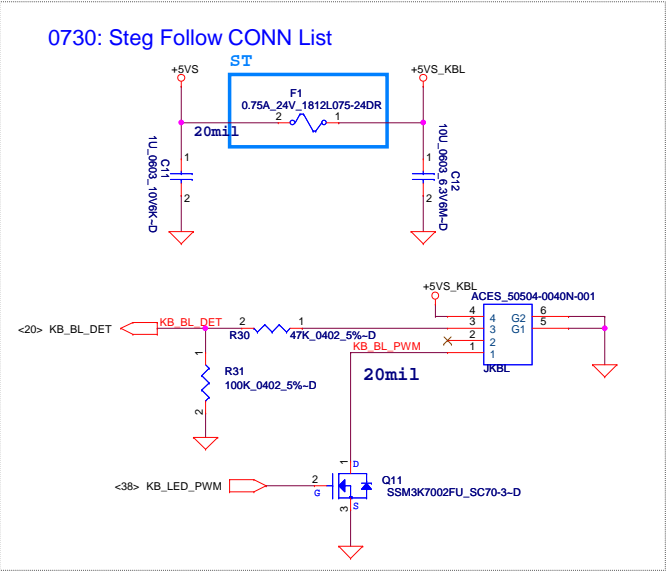


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	EC ENH-KB930/ ENE3810
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D AND TRADE SECRETARY, A DIVISION OF COMPAL ELECTRONICS, INC. NOR BE REPRODUCED OR DISCLOSED WITHOUT THE INCORPORATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				LA-7841P	Rev 0.3
				Printed: 07/27/2015	Sheet: 98 of 105

Power ON Circuit - PWR/Button Board

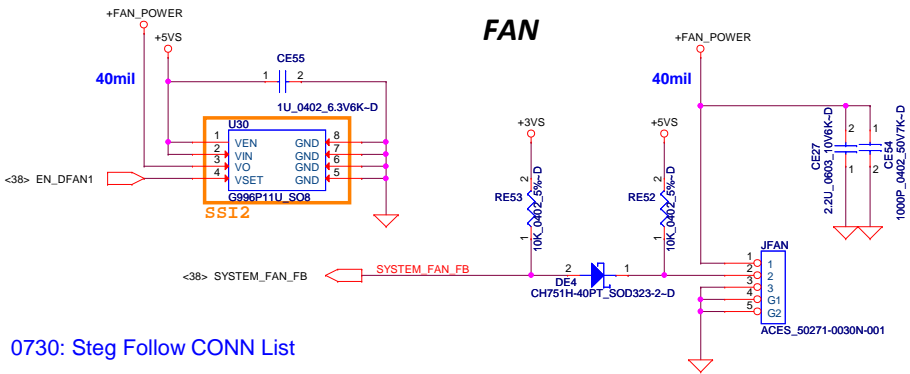


Keyboard back light

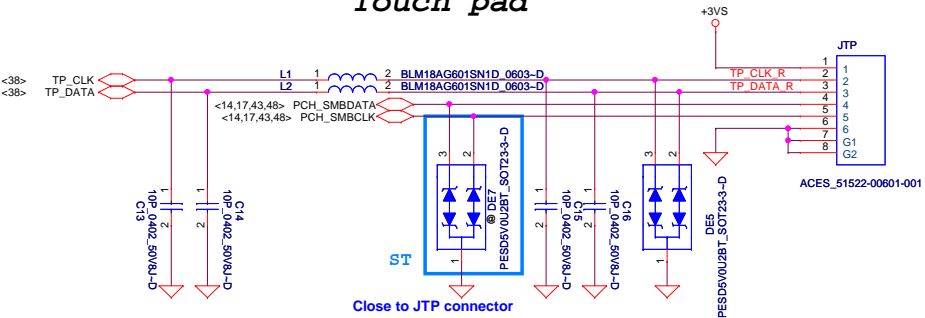


FAN Control circuit

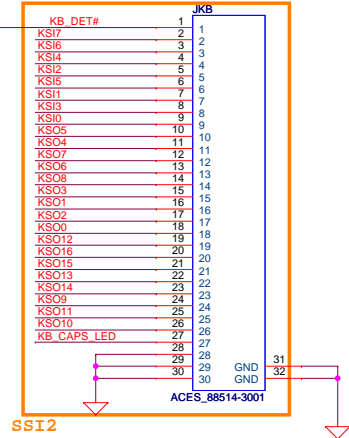
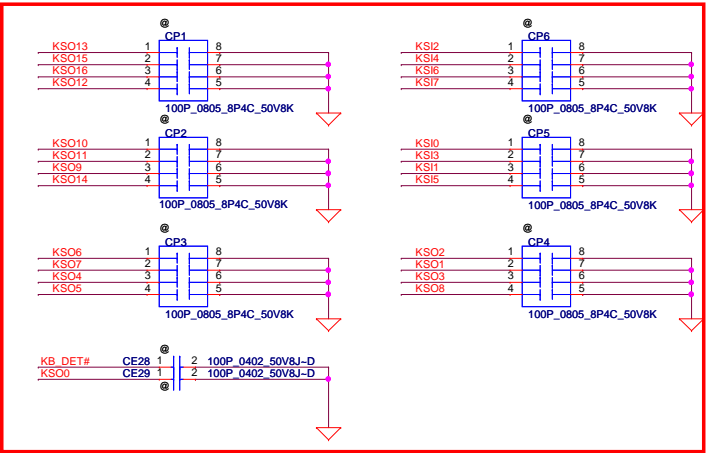
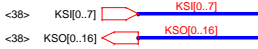
FAN



Touch pad



INT_KBD Conn.



Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	SW/TP/SCREW		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev		
				LA-7841P	0.3		
				Date:	Tuesday, February 07, 2012	Sheet	39

The schematic diagram illustrates the AT97SC3204-X2A14-AB-TSSOP28 TPM module and its connections. The central component is the AT97SC3204-X2A14-AB-TSSOP28 TPM, which is connected to various components including resistors (R1, R2), capacitors (C1, C2, C3, C4, C5, C6, C7, C8), and a 50mA current source. The diagram shows connections for VCC, V_BAT, NBO, GPIO, TEST, and NC pins. It also includes a 3V3 power supply and a 50mA current source. The diagram is labeled with 'ST' and 'U1'.

Component List:

- U1: AT97SC3204-X2A14-AB-TSSOP28 TPM
- R1: 4.7K_0402_5%-D
- R2: 33_0402_5%-D
- C1: 0.1u_0402_25V6K-D
- C2: 470p_0402_25V7K-D
- C3: 0.1u_0402_25V6K-D
- C4: 0.1u_0402_25V6K-D
- C5: 0.1u_0402_25V6K-D
- C6: 0.1u_0402_25V6K-D
- C7: 0.1u_0402_25V6K-D
- C8: 27p_0402_50V8J-D

Connections:

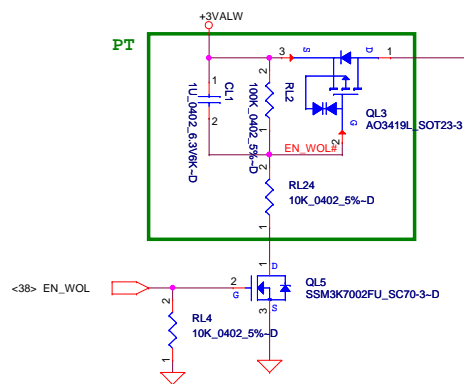
- VCC_0, VCC_1, VCC_2: Connected to +3V3.
- V_BAT: Connected to +3V3.
- NBO_13, NBO_14: Connected to +3V3.
- GPIO6: Connected to +3V3.
- TESTBI, TESTI: Connected to +3V3.
- NC_7: Connected to +3V3.
- GND_4, GND_11, GND_18, GND_25: Connected to GND.
- ATEST_1, ATEST_11, ATEST_3: Connected to GND.
- CLK_PCI_TPM: Connected to CLK_PCI_TPM.
- LPCPD#: Connected to +3V3.
- LAD0, LAD1, LAD2, LAD3: Connected to +3V3.
- LCLK, LFRAME#, LRESET#, SERIRQ, CLKRUN#: Connected to +3V3.
- TPM@C5, TPM@C6, TPM@C7, TPM@C8: Connected to +3V3.
- TPM@C1, TPM@C2, TPM@C3, TPM@C4: Connected to +3V3.
- TPM@C9: Connected to +3V3.

Diagram of a screw hole with 14 pins. The pins are arranged in two rows of seven. The top row contains pins H1, H2, H3, H4, H5, H6, and H7. The bottom row contains pins H9, H10, H11, H12, H14, H13, and H14. Pin H4 is highlighted with a purple box and labeled PT2. Each pin has a label (H1-H14), a pin number (e.g., H_2P3), and a red triangle symbol.

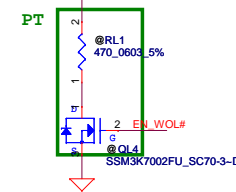
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CONN & LID Document Number LA-7841P Date: Tuesday, February 07, 2012		
				Rev 0.3 Sheet 40 of 65		

W=60mils

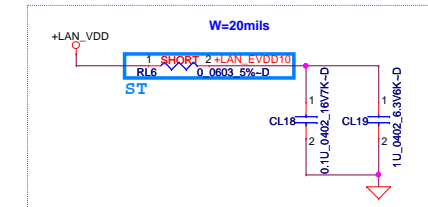
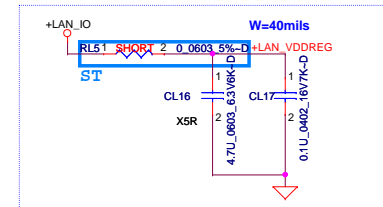
W=60mils



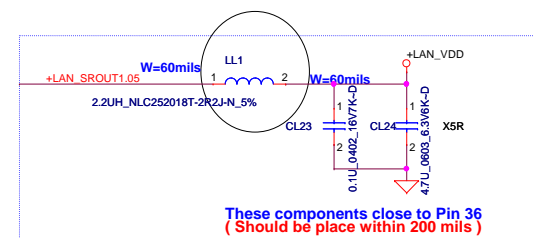
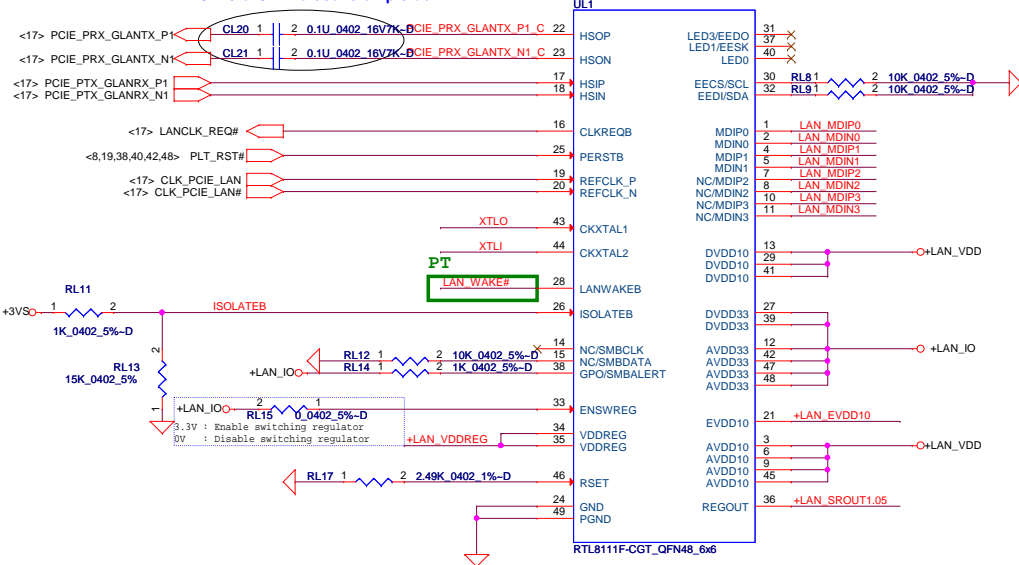
These caps close to Pin 12,27,39,42,47,48



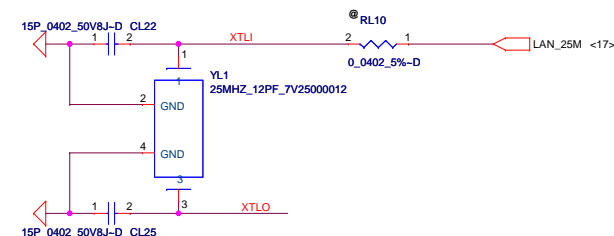
These caps close to Pin 3,6,9,13,29,41,45



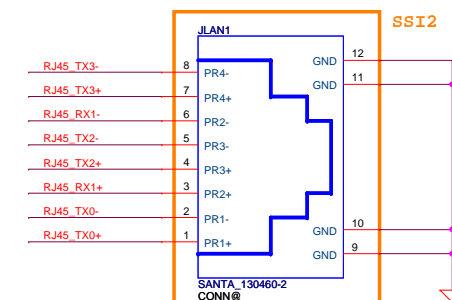
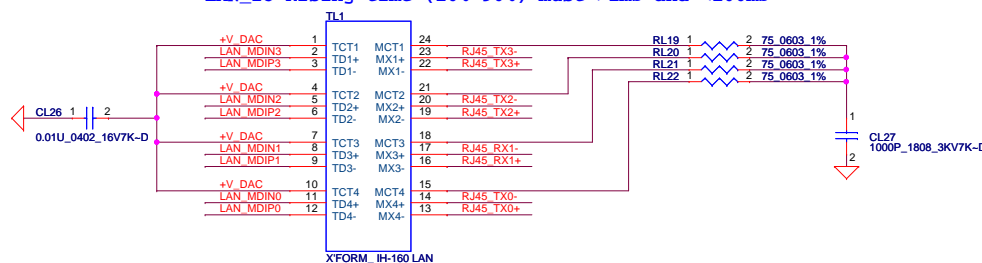
CL20 & CL21 close to chip side



These components close to Pin 36 (Should be place within 200 mils)



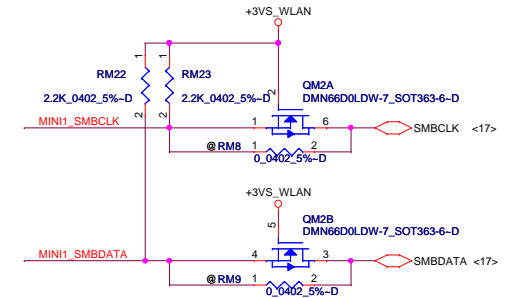
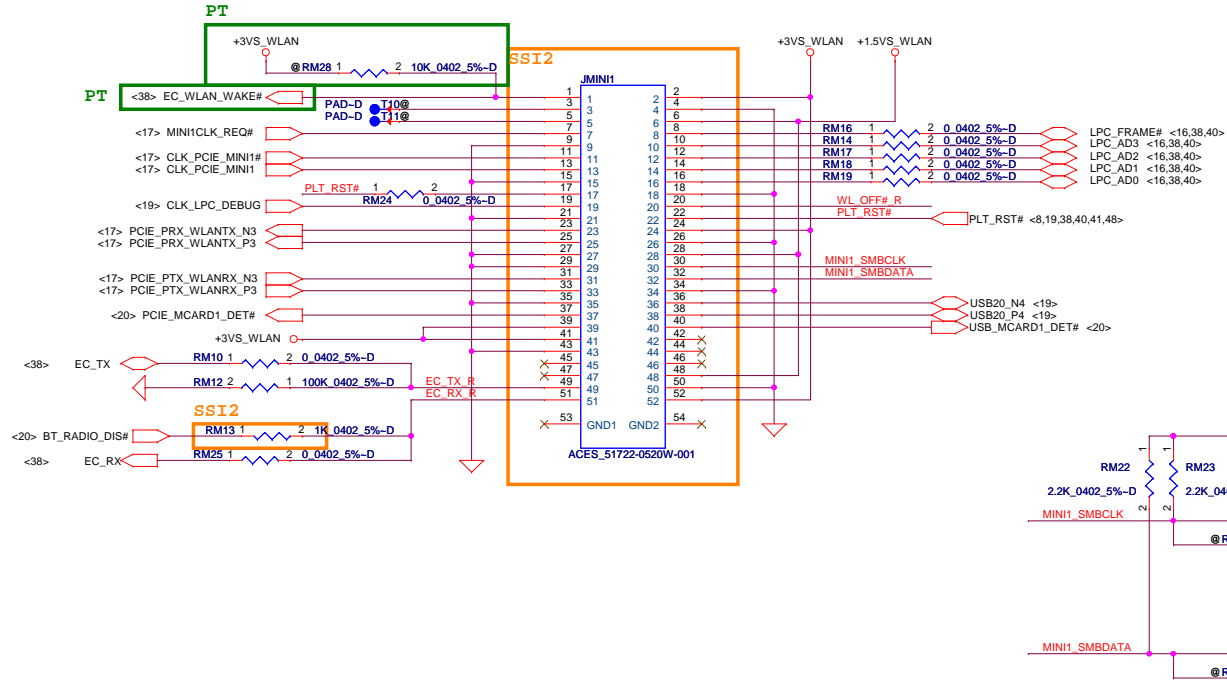
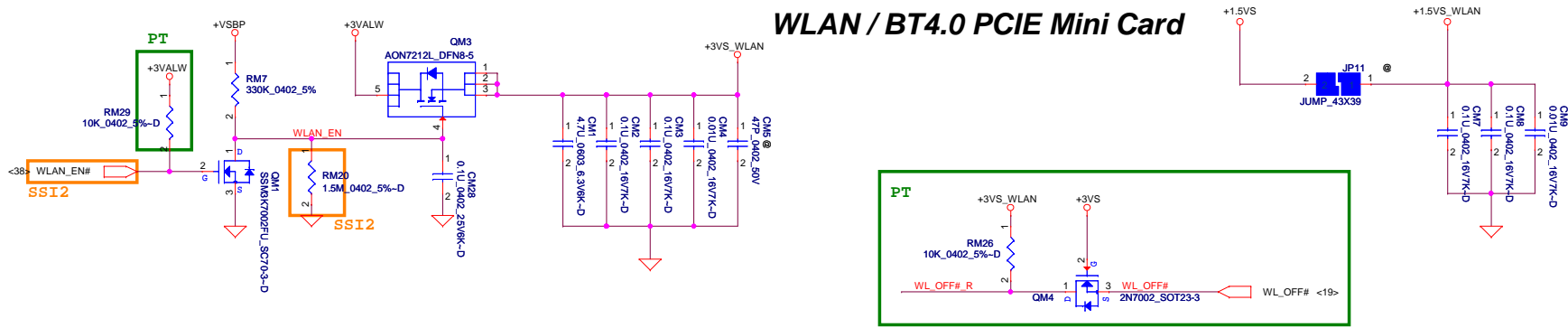
LAN_IO Rising time (10%-90%) must >1ms and <100ms



0817 Hank: Change to temp part

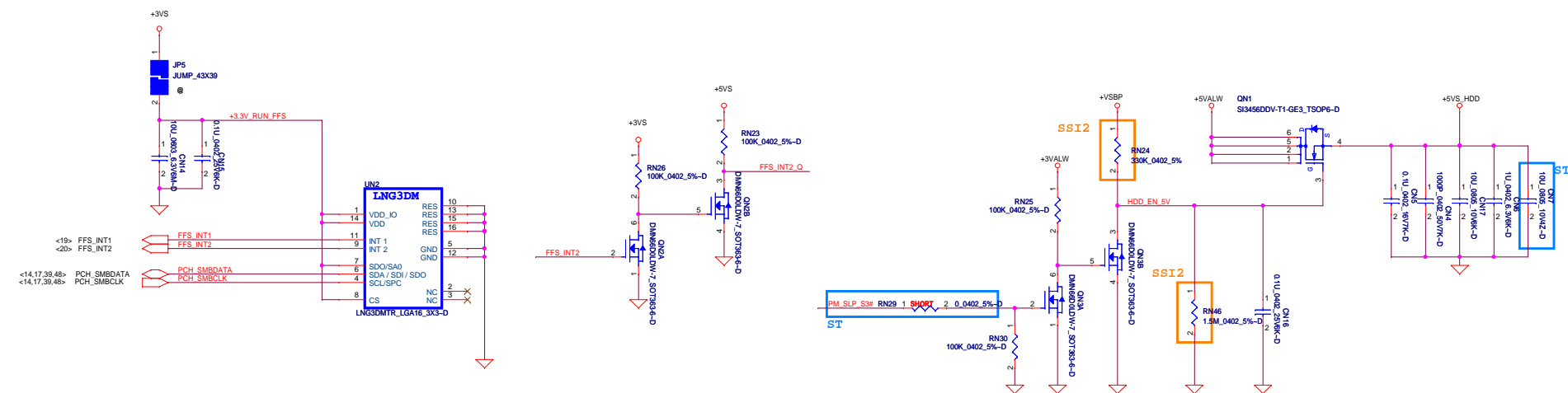
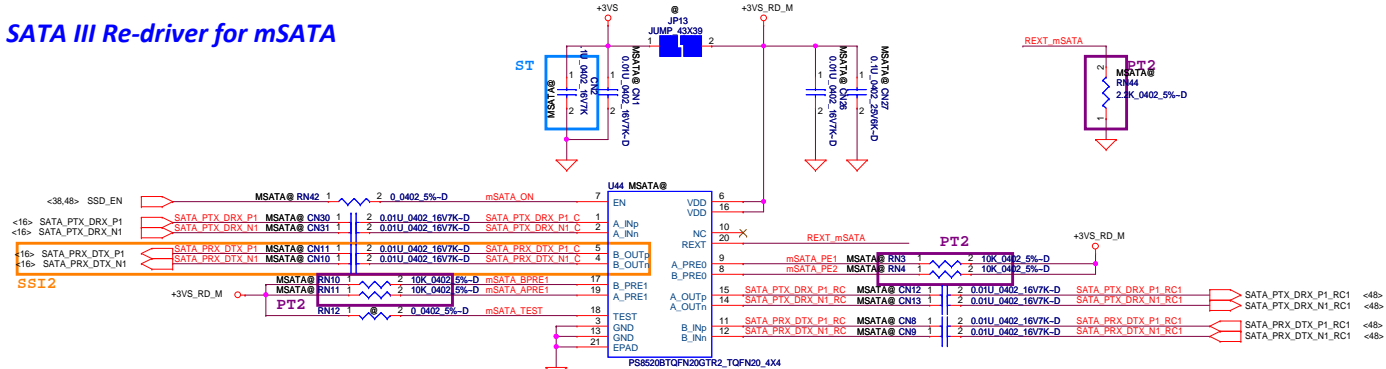
Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				P25-LAN RTL8111E	
Date: Tuesday, February 07, 2012				Sheet 41 of 65	Rev 0.3

www.teknisiindonesia.com

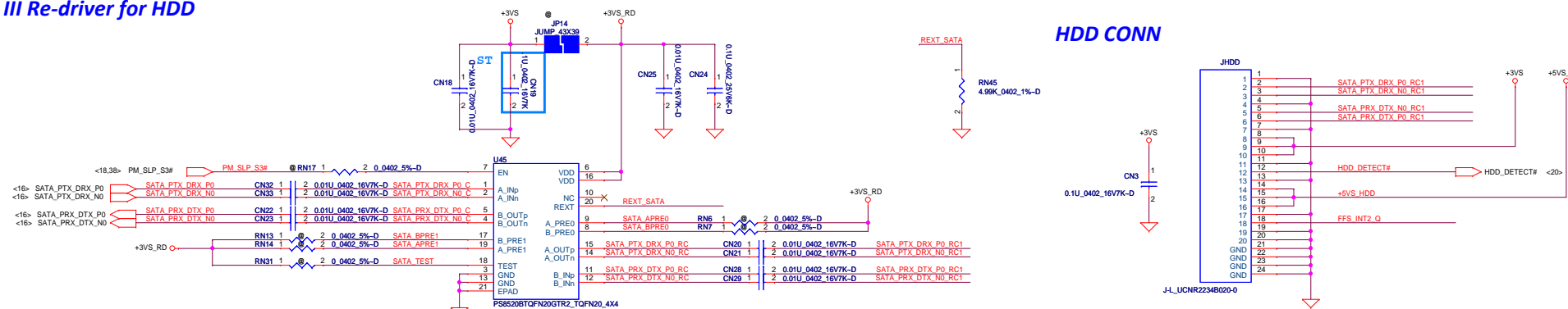
WLAN / BT4.0 PCIE Mini Card

Security Classification		Compal Secret Data		Compal Electronics, Inc. WLAN/WWAN/SIM/BT	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-7841P	Rev 0.3
Date:	Tuesday, February 07, 2012		Sheet	42	of 65

SATA III Re-driver for mSATA

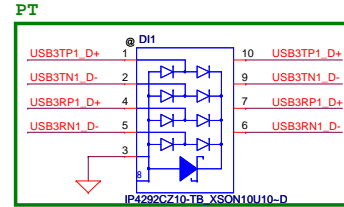
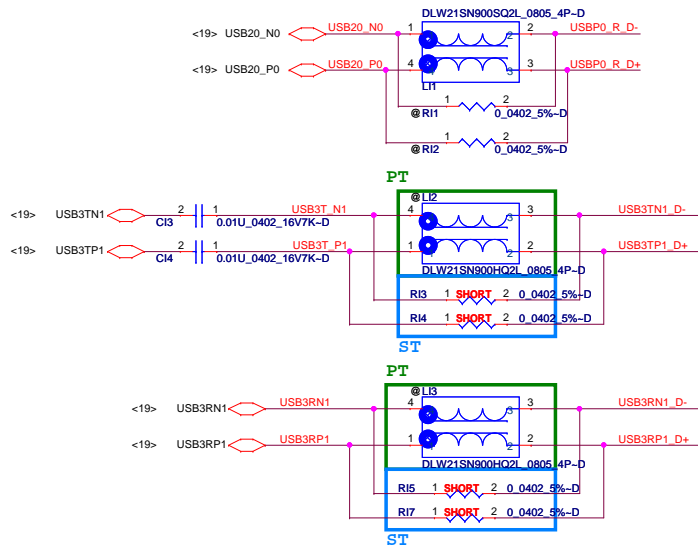


SATA III Re-driver for HDD

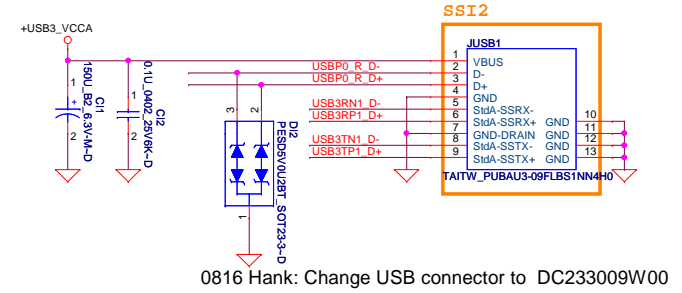


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	HDD / FFS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D AND MANUFACTURING AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number LA-7841P
					Rev D.3
				Date:	Tuesday, February 07, 2012

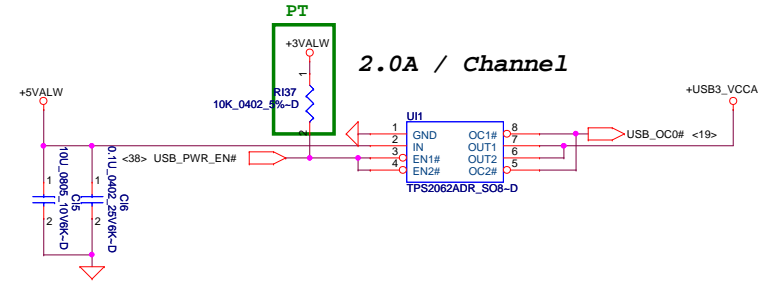
USB3.0 / USB2.0



Place close to JUSB1



2.0A / Channel

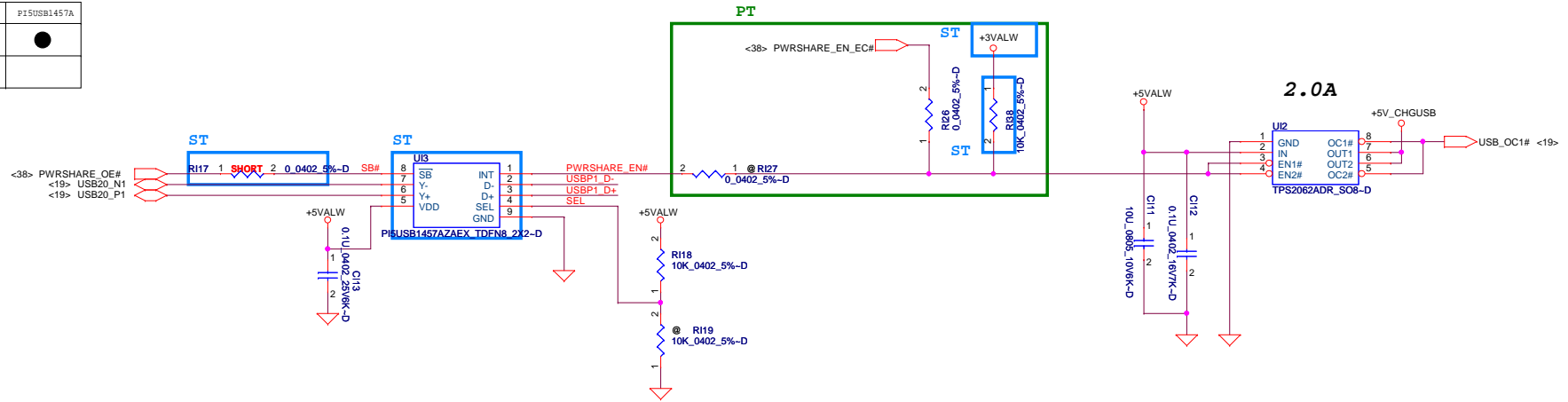


Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2011/07/15		Deciphered Date		2012/07/15	
<p>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</p>				Title			
				USB conn.			
				Document Number			
				LA-7841P			
				Date:			
				Tuesday, February 07, 2012			
Sheet				44 of 65			
Rev				0.3			

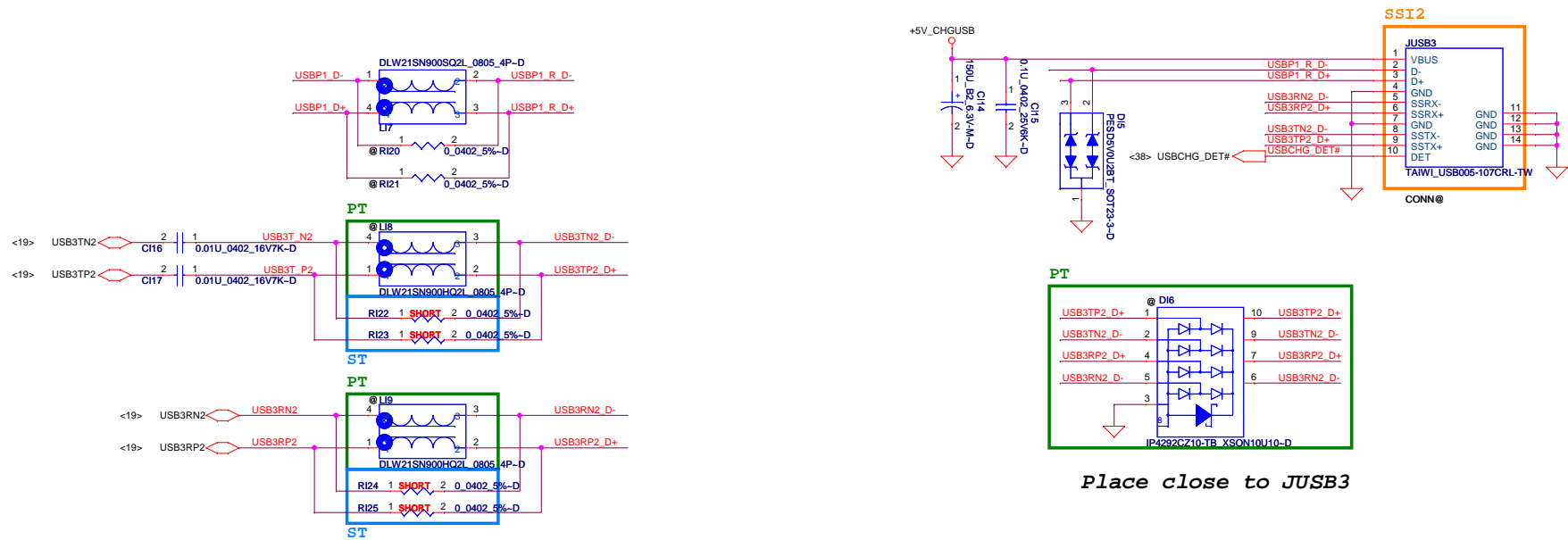
USB Powershare

	PI5USB1457	PI5USB1457A
INT		●
$\overline{\text{INT}}$	●	

USB Power Switch



USB3.0 / USB2.0



Security Classification		Compal Secret Data		Compal Electronics, Inc. USB conn.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title LA-7841P	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number LA-7841P	Rev 0.3
Date:				Tuesday, February 07, 2012	Sheet 45 of 65

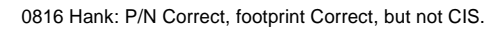


Security Classification		Compal Secret Data		Title	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	HD Audio ALC275/Audio Jack	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				Date: Tuesday, February 07, 2012	Sheet 46 of 65

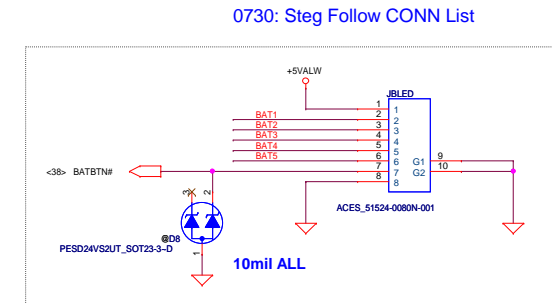
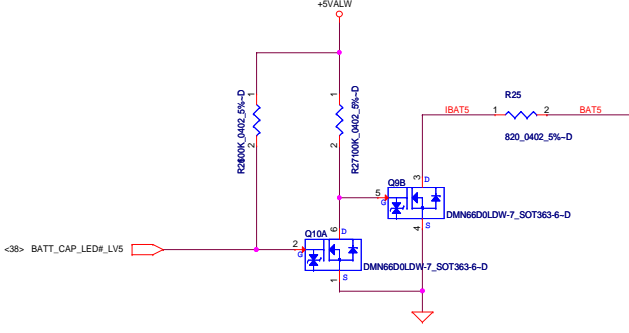
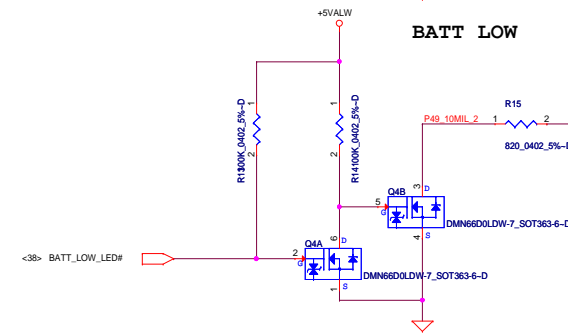
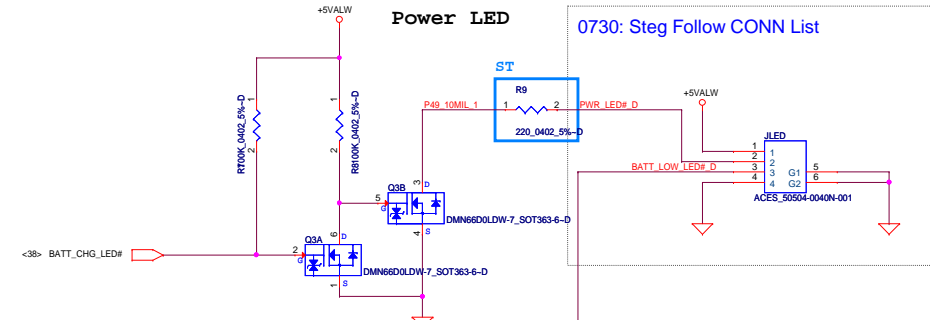
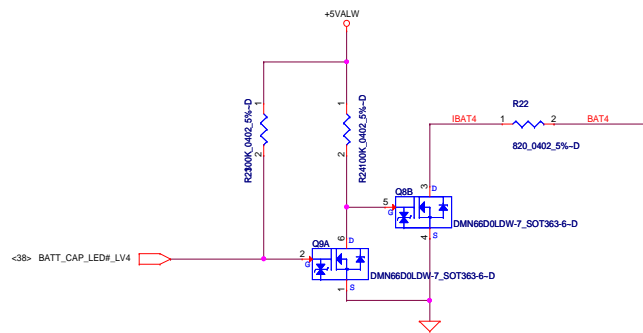
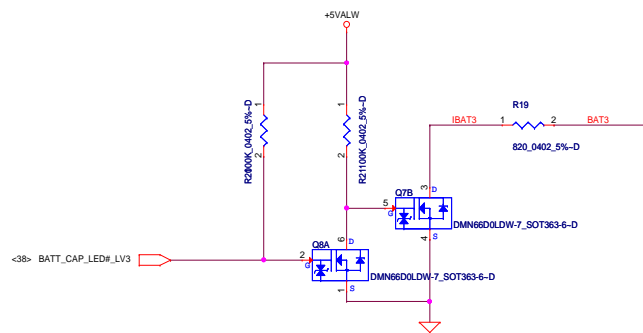
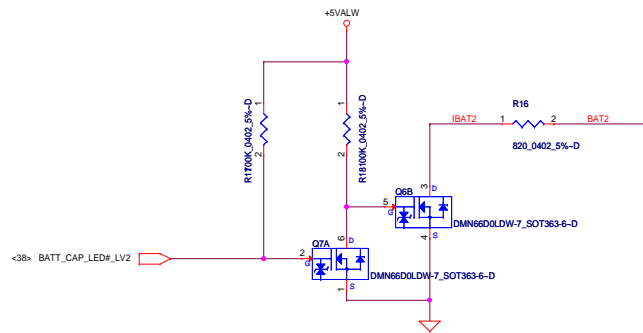
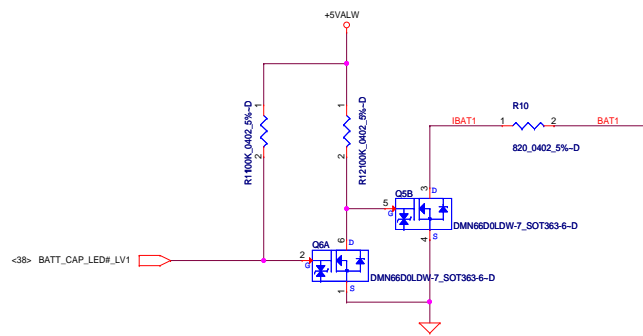


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7841P	0.3
				Date: Tuesday, February 07, 2012	Sheet 47 of 65

0730: Steg Follow CONN List



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title	Card Reader RTSS209
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RECORDS MANAGEMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.3
				LA-7841P Date: Tuesday, February 07, 2012	Sheet 48 of 65



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title	
2011/07/15		2012/07/15		Speaker/Audio Jack	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Size		Document Number	
		C		LA-7841P	
				Rev	
				0.3	
				Date: Tuesday, February 07, 2012	
				Sheet 49 of 65	

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title Block Diagram		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev 0.3
				Date:	Tuesday, February 07, 2012	Sheet 50 of 65

D

C

B

A

Title

<Title>

Size

A

Document Number

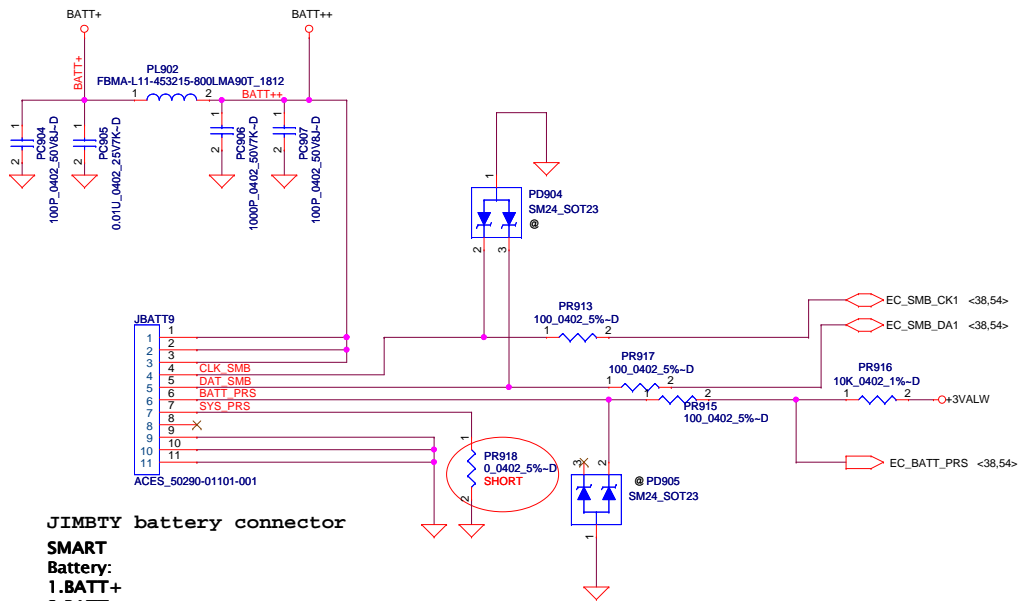
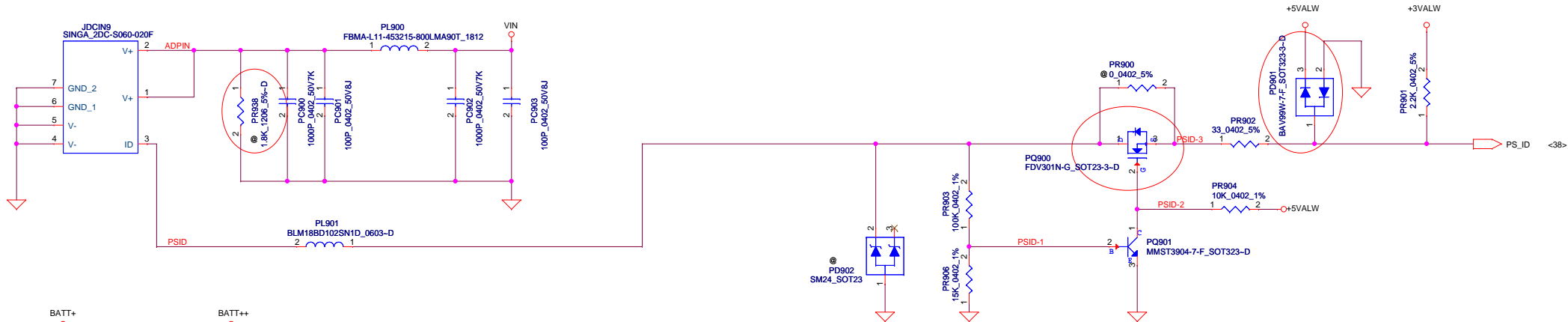
<Doc>

Rev

0.3

Date: Tuesday, February 07, 2012

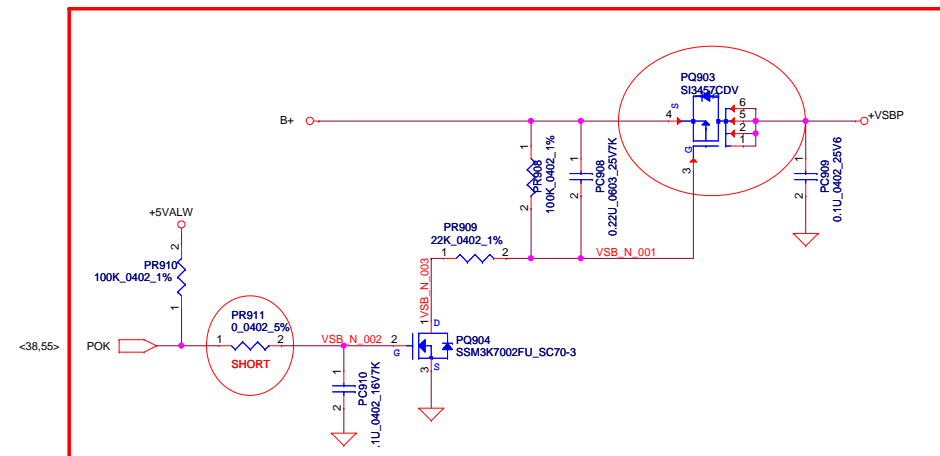
Sheet	52	of	65
-------	----	----	----



JIMBTY battery connector

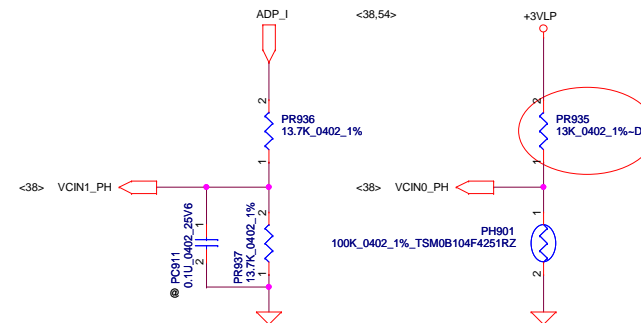
SMART Battery:

- 1.BATT+
- 2.BATT+
- 3.BATT+
- 4.CLK_SMB
- 5.DAT_SMB
- 6.BATT_PRS
- 7.SYS_PRS
- 8.BAT_ALERT
- 9.GND
- 10.GND
- 11.GND



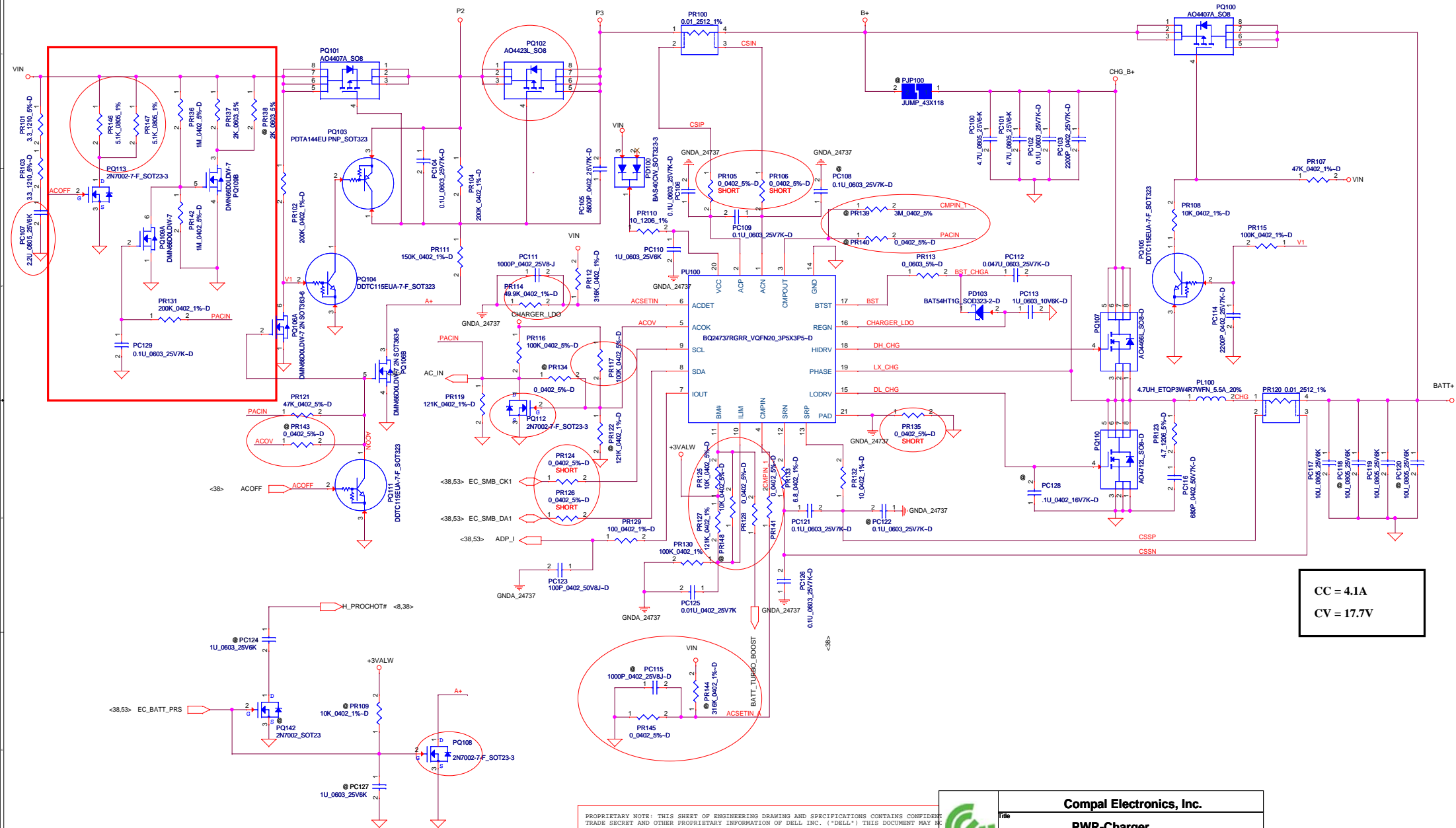
PH901 under CPU bottom side :

CPU thermal protection at 90 degree C
Recovery at 50 degree C



Iada=0~3.34A (65W)

ADP_I = 19.9*Iadapter*Rsense



CC = 4.1A
CV = 17.7V

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

Compal Electronics, Inc.			
File	PWR-Charger		
Size	Document Number	Rev	
	XPS14	0.1	
Date	Thursday, February 07, 2012	Sheet	54 of 65

3.3VALWP
TDC 7.64A
Peak Current 10.7A
OCP current 12.84A

	TYP	MAX
H/S Rds(on)	:27mohm	34mohm
L/S Rds(on)	:11mohm	14mohm

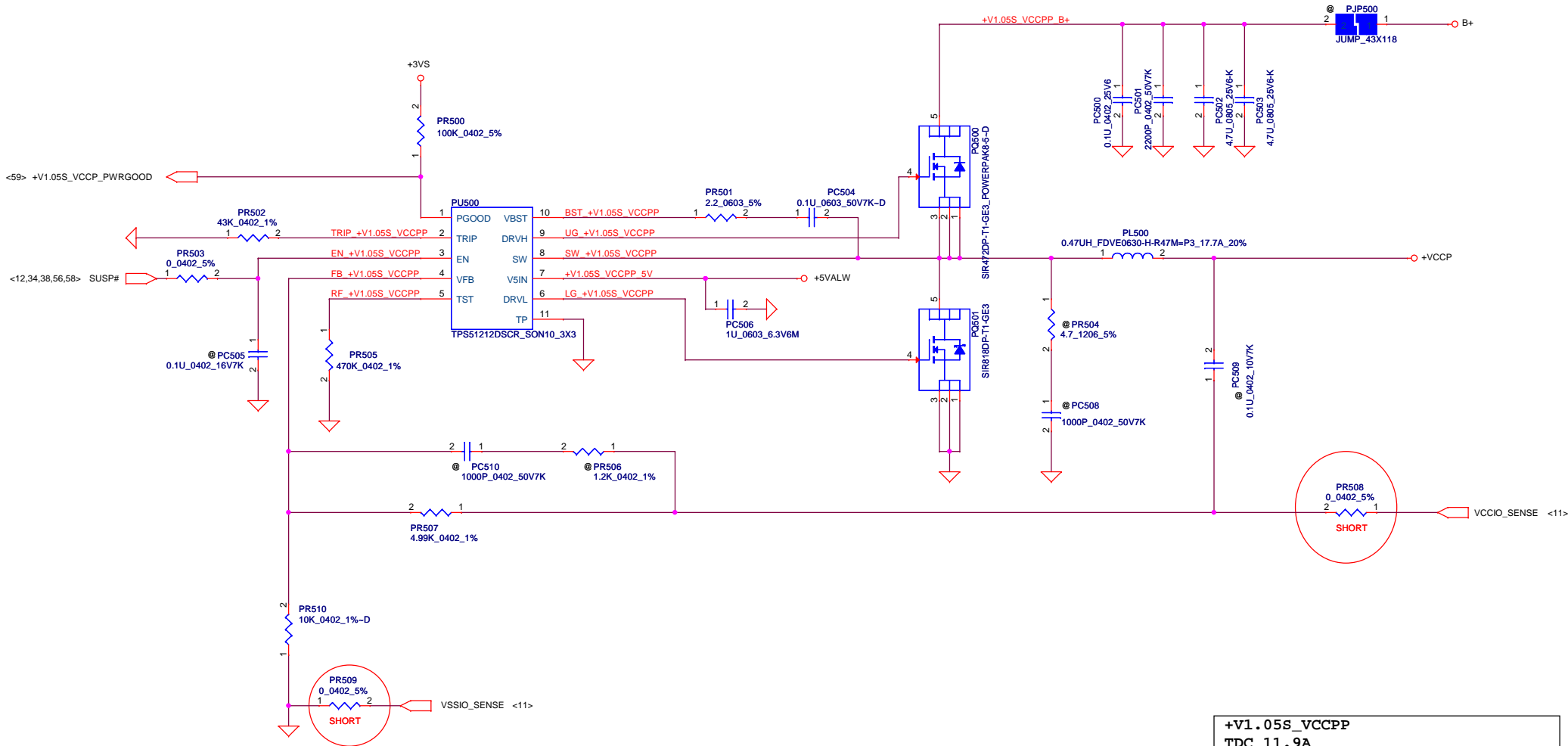
5VALWP
TDC 4.54A
Peak Current 6.49A
OCP current 7.788A

	TYP	MAX
H/S Rds(on)	:27mohm	34mohm
L/S Rds(on)	:11mohm	14mohm

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



Compal Electronics, Inc.			
Title			
PWR-3VALWP/5VALWP			
Size	Document Number	Rev	
		XPS14	
Date:	Tuesday, February 07, 2012	Sheet	55 of 65



+V1.05S_VCCPP	
TDC 11.9A	
Peak Current 17A	
OCP current 20.4A	
	TYP MAX
H/S Rds(on) :	10mohm , 14.5mohm
L/S Rds(on) :	3mohm , 3.6mohm

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



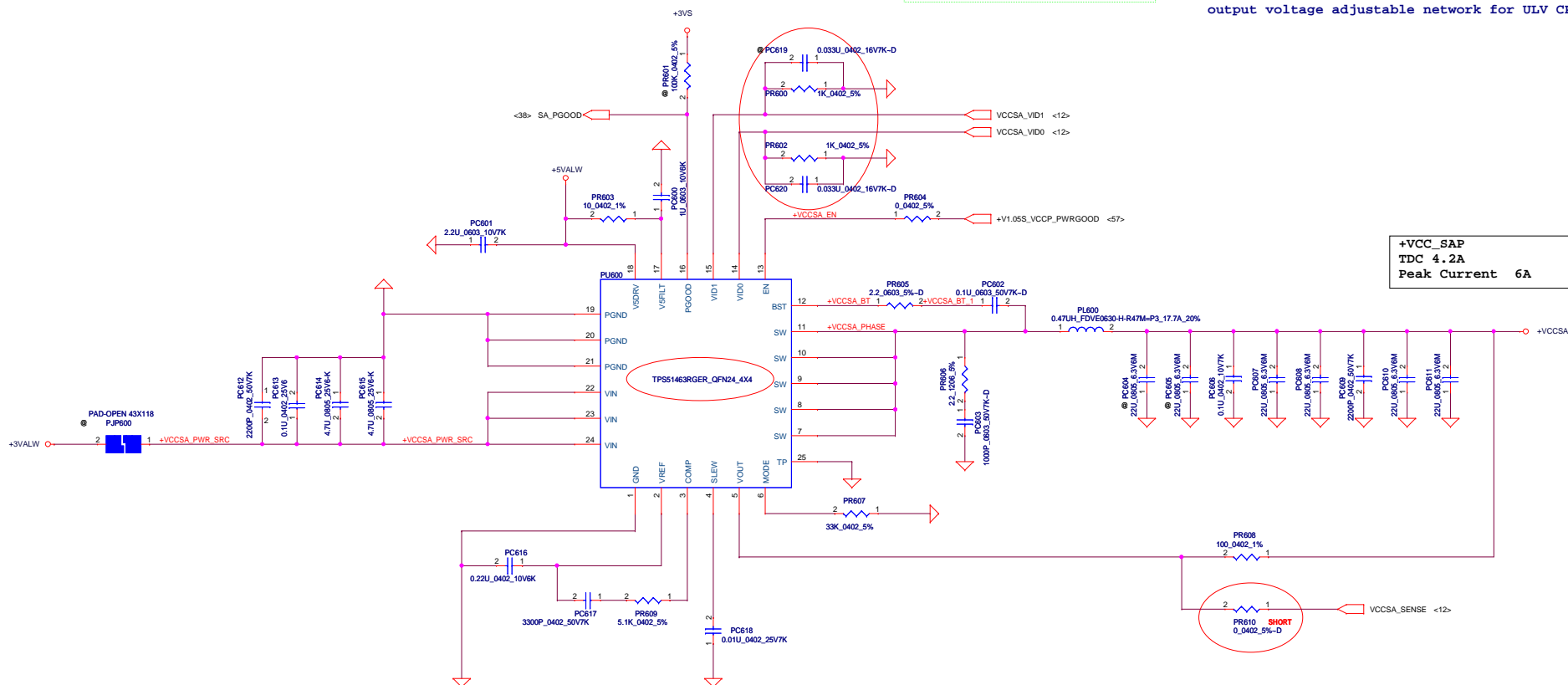
Compal Electronics, Inc.

Title		PWR-V1.05S_VCCPP	
Size	Document Number	XPS14	
Date	Tuesday, February 07, 2012	Sheet	57 of 65
Rev	0.1		

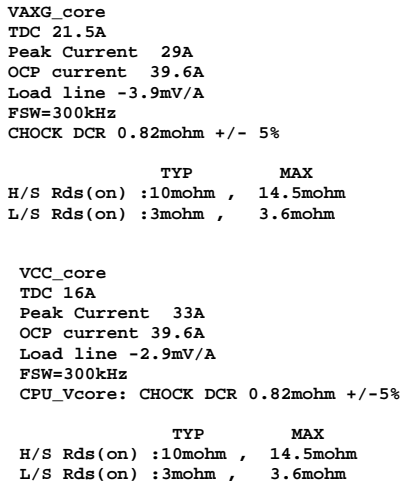
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

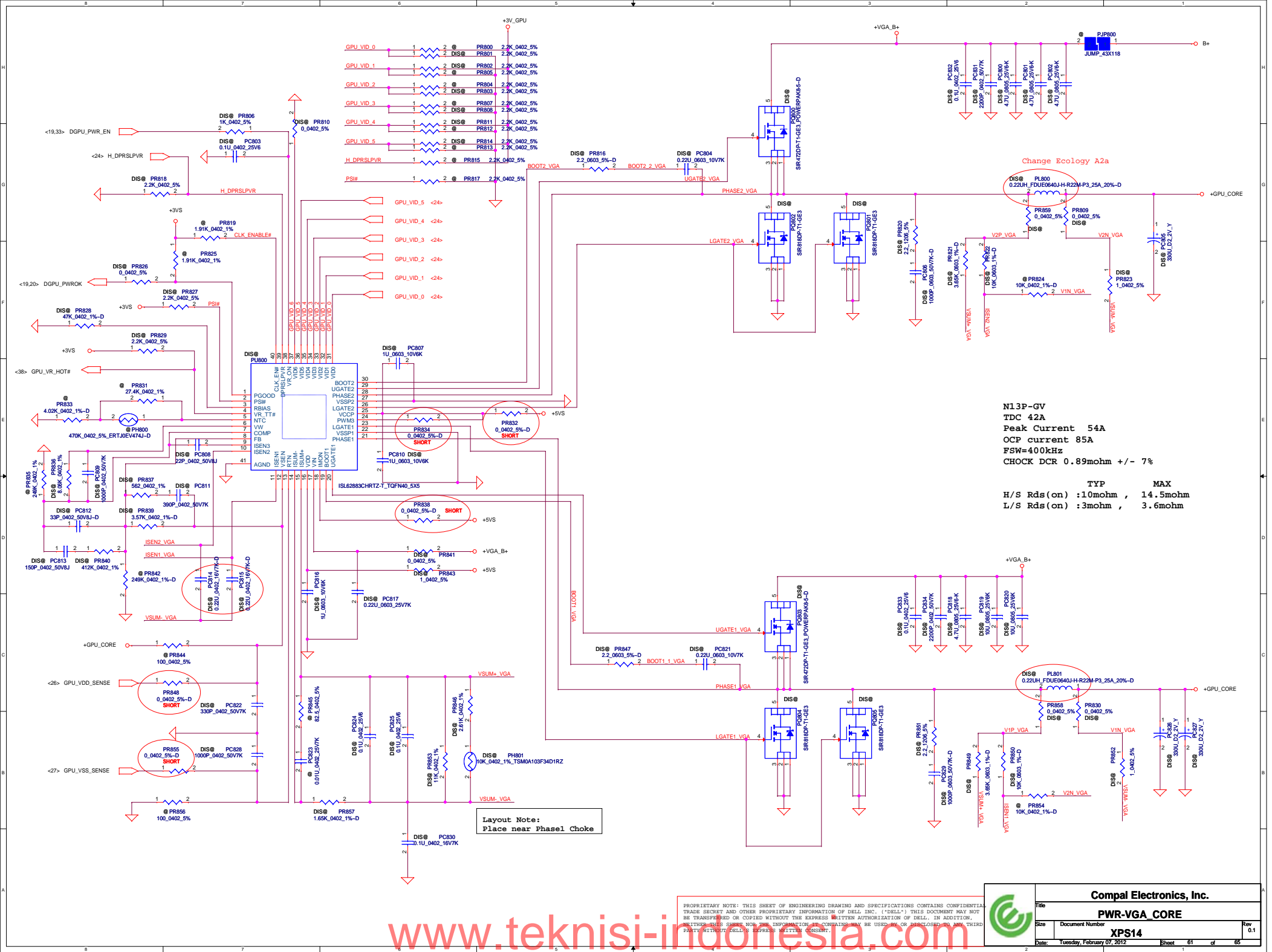
output voltage adjustable network for ULV CPU

The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.




+VCC_SAP
TDC 4.2A
Peak Current 6A

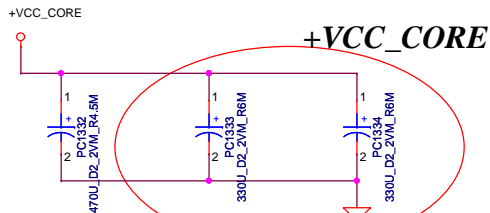
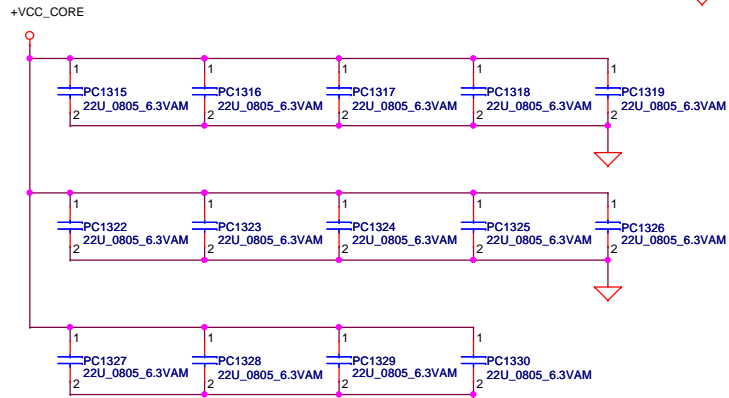
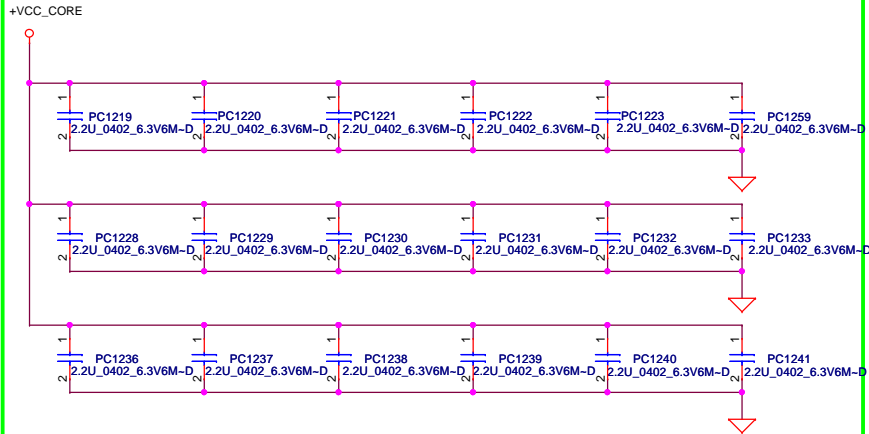




PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSMITTED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

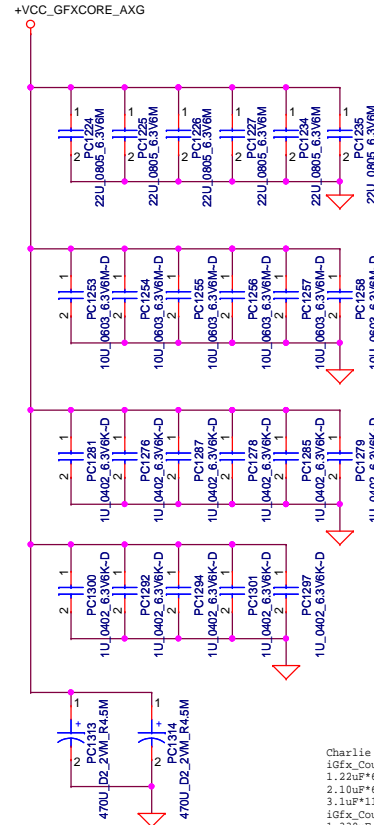
		Compal Electronics, Inc.	
		PWR-VGA_CORE	
Size	Document Number	XPS14	
Date	Tuesday, February 07, 2012	Sheet	61 of 65

+VCC_CORE



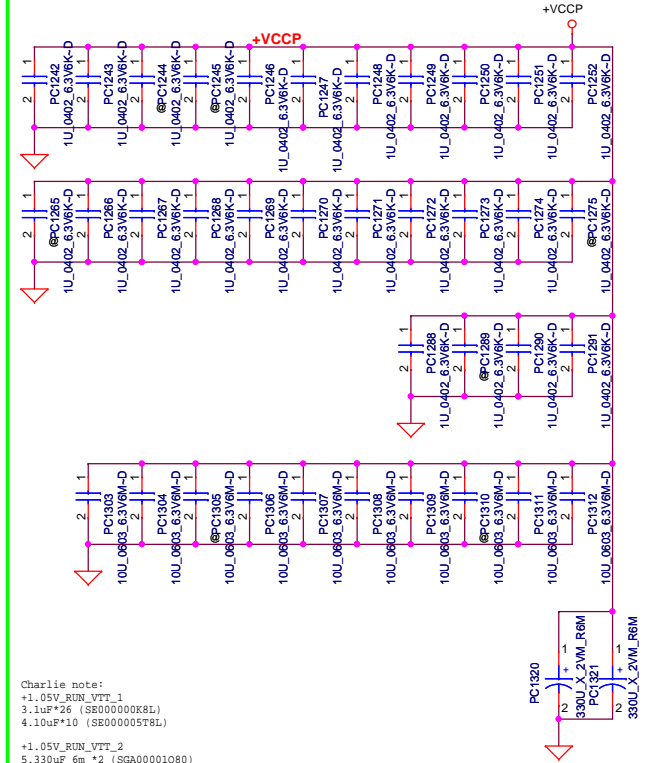
Charlie note: Vcore_Cout1
1.2.2uF*16 (SE00000888L)
2.22uF*12 (SE000008180)
Vcore_Cout2
1.330uF 9m *3 (SGA20331E10)

+VCC_GFXCORE_AXG



Charlie note: iGfx_Cout1
1.22uF*6 (SE000000110)
2.10uF*6 (SE00000578L)
3.1uF*11 (SE000000K8L)
iGfx_Cout2
1.330uF 9m *2 (SGA20331E10)

+VCCP



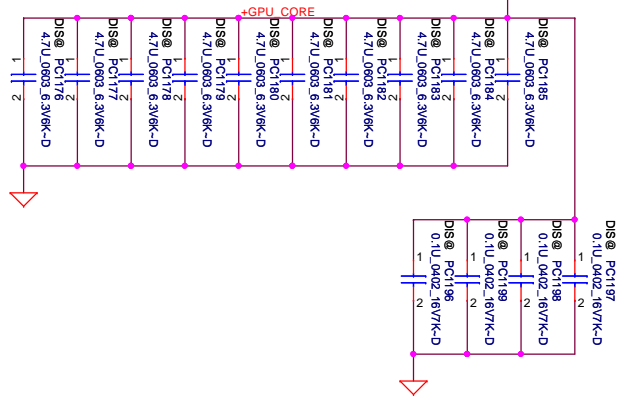
Charlie note: +1.05V_RUN_VTT_1
3.1uF*26 (SE000000K8L)
4.10uF*10 (SE00000578L)
+1.05V_RUN_VTT_2
5.330uF 6m *2 (SGA00001Q80)



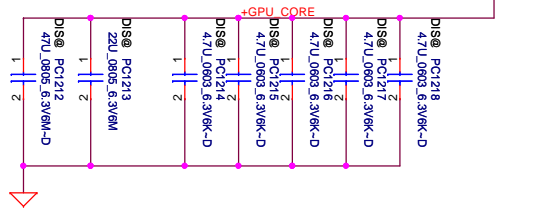
Compal Electronics, Inc.

Title		
PROCESSOR DECOUPLING		
Size	Document Number	Rev
	XPS14	0.1
Date:	Tuesday, February 07, 2012	Sheet 62 of 65

+GPU_CORE (place under GPU)



+GPU_CORE (place near GPU)



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Compal Electronics, Inc.			
Title		GPU DECOUPLING	
Size	Document Number	Rev	
	XPS14	0.1	
Date:	Tuesday, February 07, 2012	Sheet	63 of 65

D

BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION,
NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD
PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

3

C

B

A

		5		4		3		2		1
Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description		Solution Description	
QLM00	1	38	01/12			1.0	PCB REV change to 1.0		Change RE77 to 56K	
	2	24	01/12			1.0	Change EC_SMB_CK2_PX/EC_SMB_DA2_PX pull up resistor as design guide		Change RV2420,RV2421 to 2.2K	
	3	39	01/12			1.0	Adjust CAPS_LED brightness		Change RE84 to 470ohm	
	4	45	01/12			1.0	Sync up with XPS 15" for pull up power rail		RI38 pull up from +5VALW to +3VALW	
	5	17,24,35	01/12			1.0	Solve adaptor detect issue		Depop QH3; change GPU SMBus/Ambient Light Sensor connect to PCH_SMLDATA and PCH_SMLCLK	
	6	45	01/12			1.0	Purchase recommend		Change UI3 to high active parts	
	7	40	01/12			1.0	BOM structure control		ADD TPM@ for TPM circuit	
	8	38	01/12			1.0	For USBCHG_DET_D can't turn on 3V/5V issue		Change RE78 pull up to +3VLP	
	9	45	01/12			1.0	Vendor recommend		UI2 EN pin pull up resistor RI38 change to 10K	
	10	35	01/12			1.0	Change JLVDS connector PN and footprint as assembly issue		Change JLVDS connector PN to SP01001BT00, footprint to ACES_59003-04006-001_40P	
	11	39	01/12			1.0	ME change		SW1 PN change to SN100005100	
	12	33	01/16			1.0	Solve 1.5V voltage drop issue		Change QV2803 to SB00000SJ0L to lower Rds on	
	13		01/16			1.0	Remove 0 ohm to short pad for MP		RI22,RI23,RI24,RI25,RI17,RI3,RI4,RI5,RI7,RN29,RM10,RM25,RL25,RL6,R34,RE83, RE10,RE34,RE35,RE39, RE68,RE70,RE71,RE60,RE62,RE63,RE64,RV449, RV3519,RV3517,RI6,RI8,RV3525,RH199,RH105,RH106,RH108,RH110,RH112,RH101, RH103,RH107,RH44,RU125,RU122,RU123,RU116,RU131,RU75,RU62	
	14	10	01/17			1.0	Change setting for Ivy Bridge support 1x16 PCI Epress and Sandy Bridge only UMA Config		Depop RU85	
	15	49	01/17			1.0	ME requirement for LED brightness tuning		R9 Change to 220ohm for Power LED(White)	
	16	39	01/18			1.0	EMI requirement		Add DE7 on TP SMBus	
	17	38,35,39	01/19			1.0	Thailand flood disaster, original material shortage		Change DE1,DE2,DE3,DE6 PN to SCS00002G00; QE5,QE6,QV3508,QZ10,QZ13,QZ15 to SB00000M700; DV9 to SCS00002G00	
	18	35	01/19			1.0	JLVDS pin define change for opertion risk		JLVDS Pin38 NC and up shift to Pin33	
	19	33	01/20			1.0	Change HF part		Change RZ10,RZ11,RZ40,RZ41 PN to SD028220A8L	
	20	48	01/20			1.0	Manufacture highlight change		Change JSATA footprint to ACES_50463-0104A-001_10P-T	
	21	17,19,40	01/20			1.0	EMI requirement		Populate PCI CLK reserved parts RH65,CH26,CH31,R2,C8	
	22	36	01/20			1.0	EMI requirement for LVDS		Change LV7,LV8,LV9,LV10 to SM070002S00	
	23	39	01/30			1.0	Change HF part		Change F1 to SP040003200	
	24	48,53	01/30			1.0	Solve audio power consumption issue		Change PQ903 PN to SB93457001L, JSATA pin8 B+ change to +VSBP	
	25	17,38	01/30			1.0	EMI requirement		Populate CH98,CE11,RE13	
	26	14	02/01			1.0	1.5V power rail reach up to 1.614V, change for derating concern		CD7 capacitor change from 2V to 2.5V	
	27	15	02/02			1.0	EMI requirement		Add RV3529,RV3530,CV3528,CV3529	
	28		02/02			1.0	Customer concern Y5V MLCC performance		Change CA59 to SE076104K80; CE17 to SE064475KL0;CN2,CH11,CN19,CM25,CM26, CM29,CU33,CU34,CU35,CU36,CU97,CU155 to SE076104K80; CM24,CU39 change to SE076473K80; CN7,CZ11,CV3508 change to SE064106M8L	
	29									
	30									
	31									
	32									